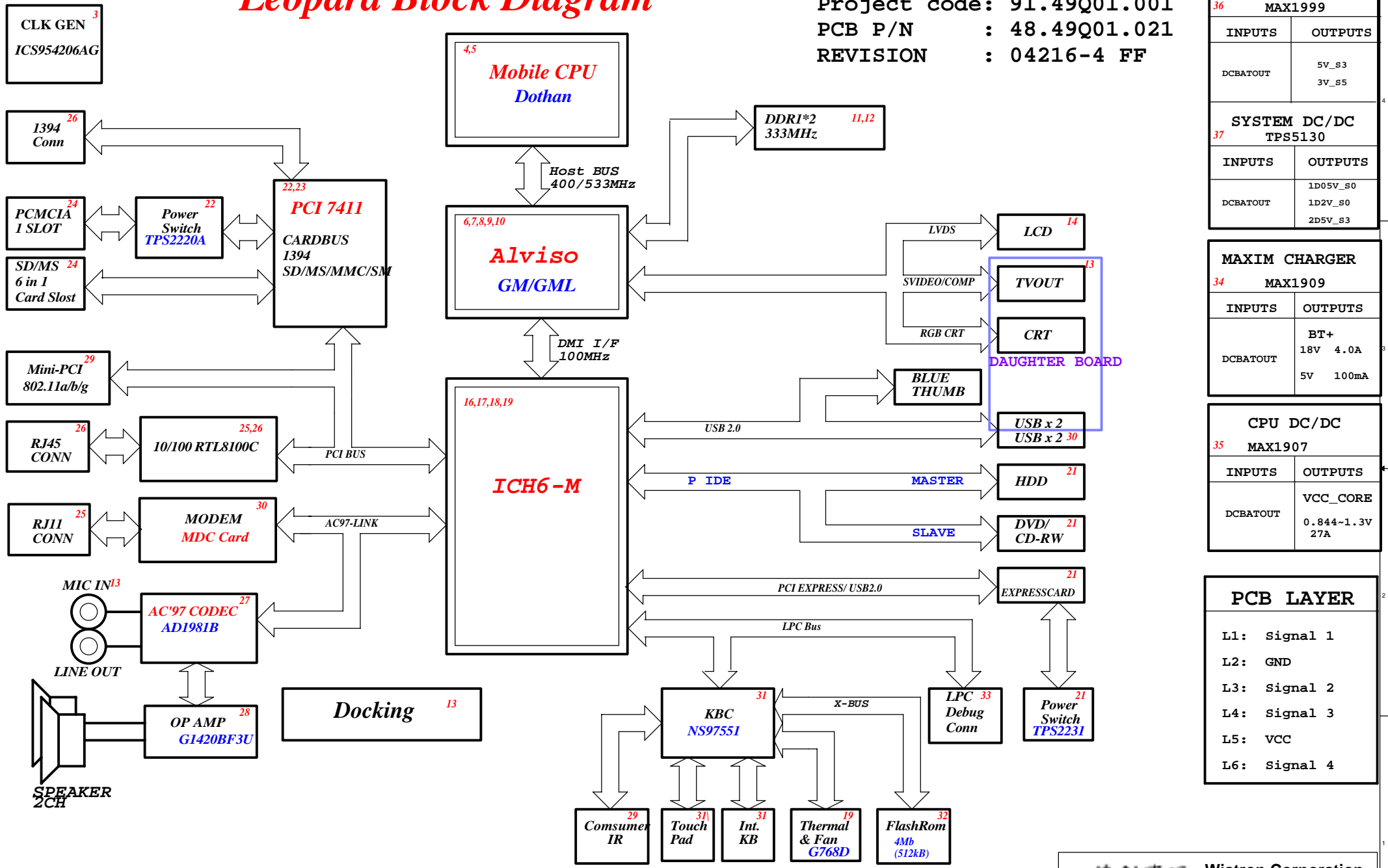


# Leopard Block Diagram

Project code: 91.49Q01.001  
 PCB P/N : 48.49Q01.021  
 REVISION : 04216-4 FF



SYSTEM DC/DC MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **Leopard** Rev: -4

Date: Sunday, February 27, 2005 Sheet 1 of 41

# ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

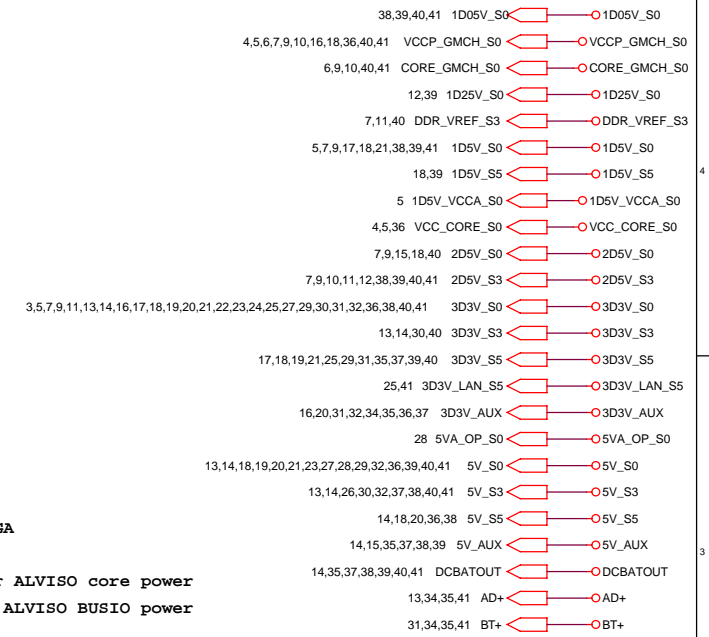
# ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

# Power name description

5V\_S0= 5 Voltage power up on system work(S0 state)  
 5V\_S3= 5 Voltage suspend to RAM(S3 state)  
 5V\_S5= 5 Voltage soft off(S5 state)  
 3D3V\_S0= 3.3 Voltage power up on system work(S0 state)  
 3D3V\_S3= 3.3 Voltage suspend to RAM(S3 state)  
 3D3V\_S5= 3.3 Voltage soft off(S5 state)  
 LVDDR\_2D5V= 2.5 Voltage power up on system work(S0 state)  
 2D5V\_S3= 2.5 Voltage suspend to RAM(S3 state)  
 2D5V\_S0= 2.5 Voltage power up on system work(S0 state)

VCC\_CORE\_S0= CPU VID Voltage power up on system work(S0 state)  
 1D5V\_VCCA\_S0= 1.5 Voltage power up on system work(S0 state)  
 1D5V\_S0= 1.5 Voltage power up on system work(S0 state)  
 1D5V\_S5= 1.5 Voltage soft off(S5 state)  
 DDR\_VREF\_S3= 1.25 Voltage suspend to RAM(S3 state)  
 1D25V\_S0= 1.25 Voltage power up on system work(S0 state)  
 1D2\_VGA\_S0= 1.2 Voltage power up on system work(S0 state) for VGA  
 1D05V\_S0= 1.05 Voltage power up on system work(S0 state)  
 CORE\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power  
 VCCP\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power



# PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS) P_INTG# (1394) P_INTF# (CARD READER) P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

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Title: **ITP**

Size: A3	Document Number: <b>Leopard</b>	Rev: <b>-4</b>
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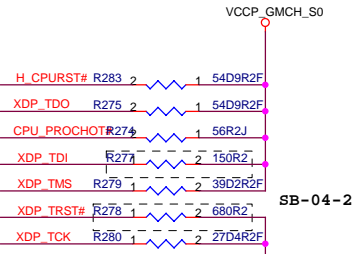
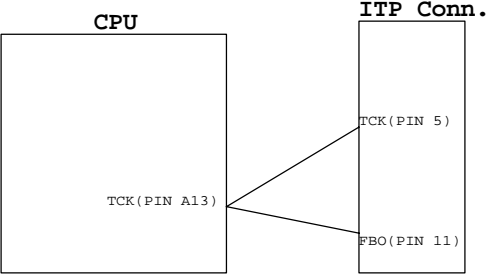
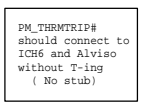
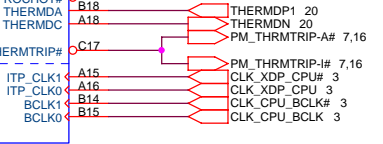
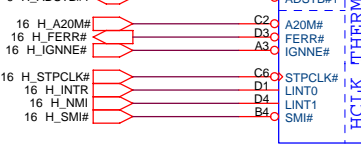
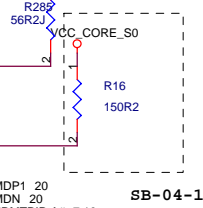
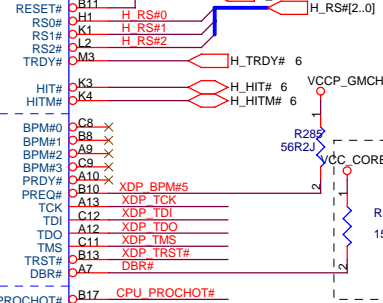
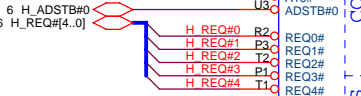
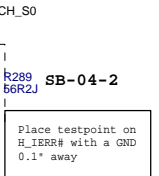
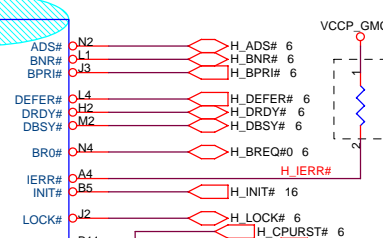
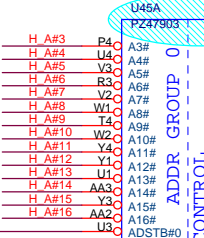
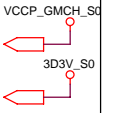
Date: Sunday, February 27, 2005 Sheet 2 of 41



6 H\_A#[31..3]

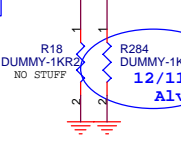
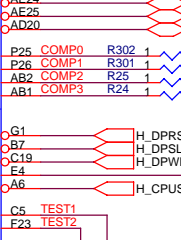
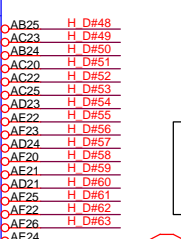
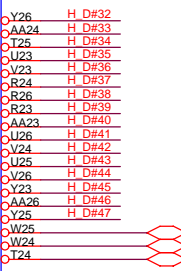
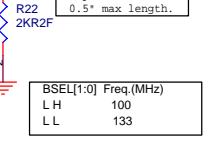
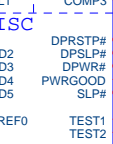
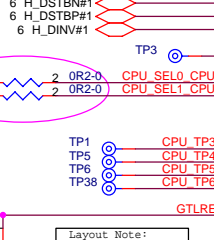
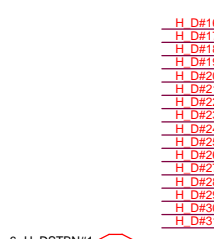
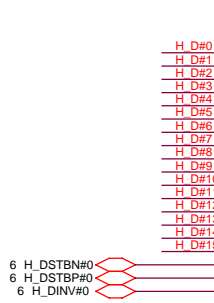
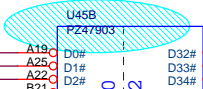
SD 0817

3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V\_S0



SB-04-2

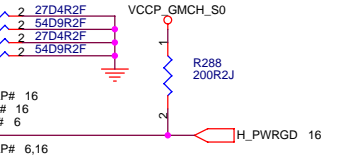
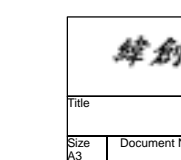
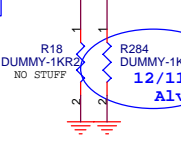
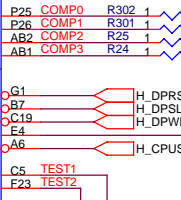
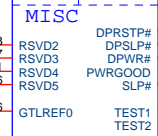
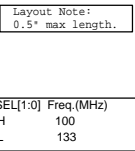
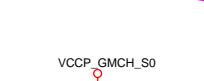
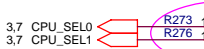
SD 0817



H\_D#[63..0] 6

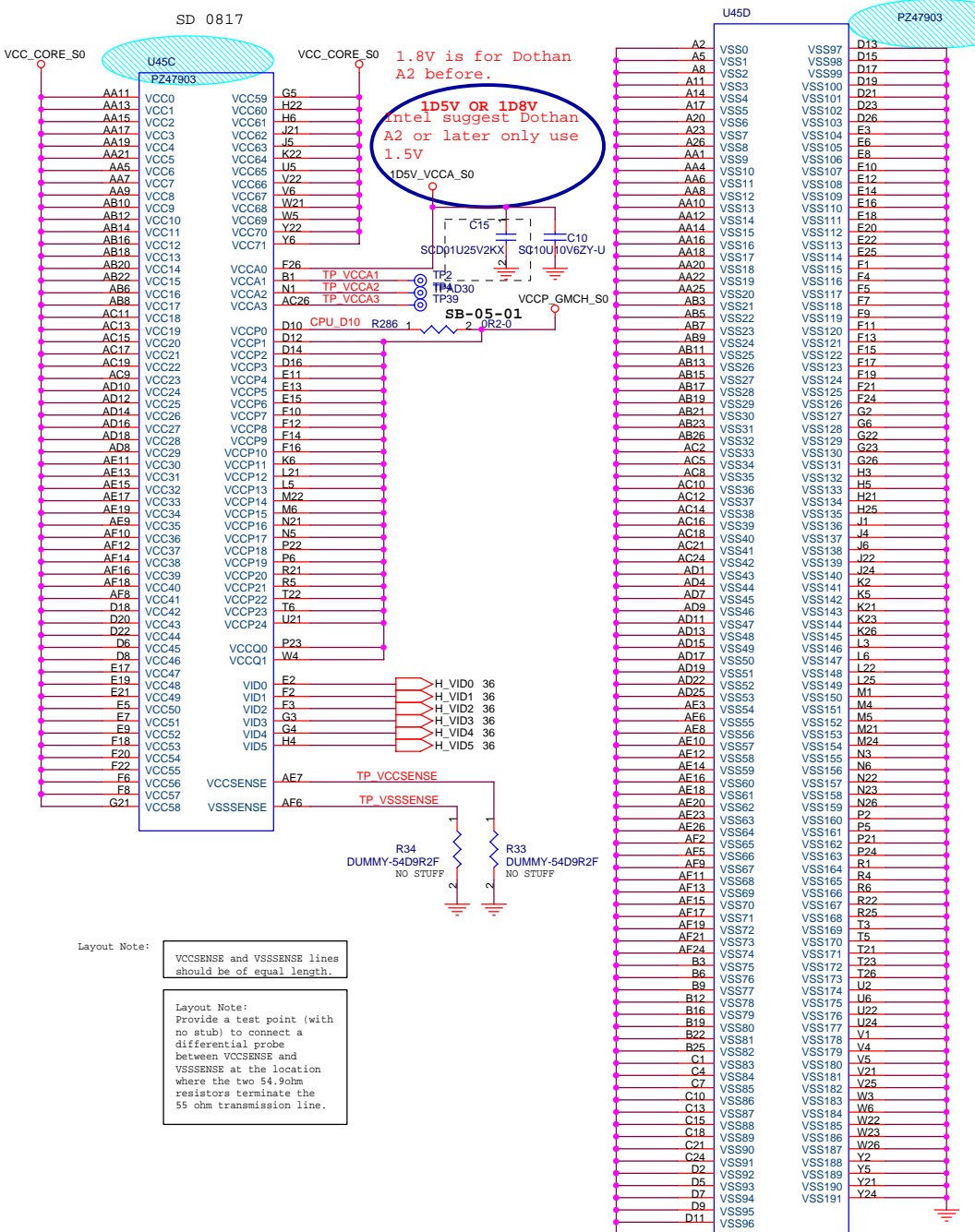
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Dothan A: R43,R44=DUMMY Dothan B: R43,R44=0R



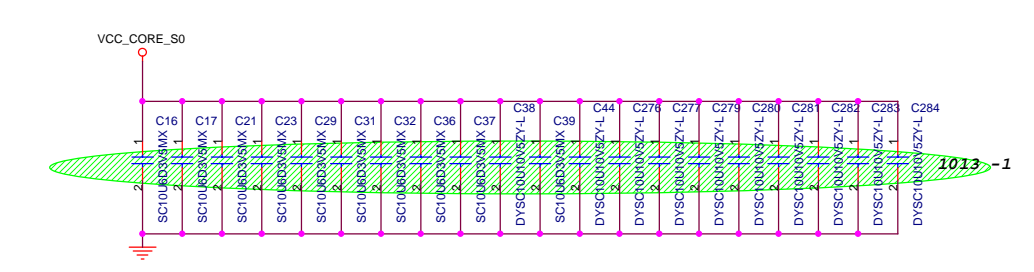
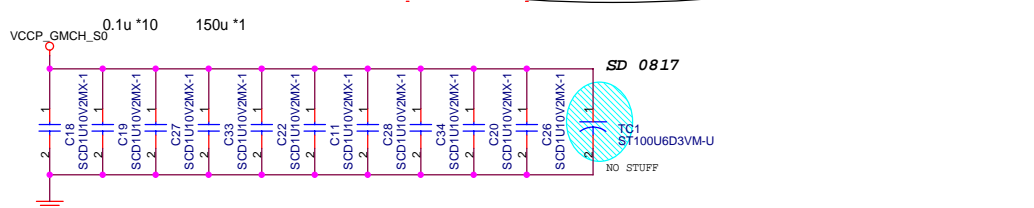
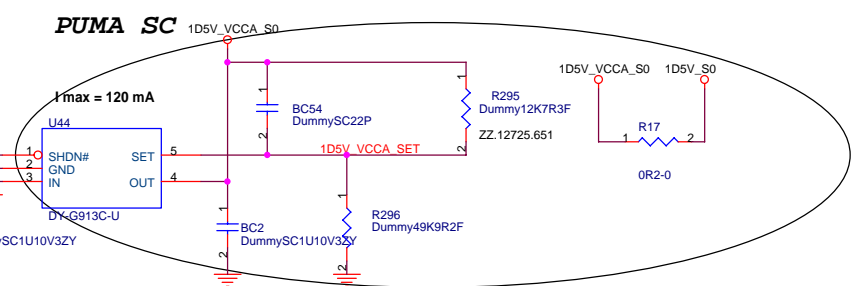
Wistron Corporation logo and title block: CPU (1 of 2), Leopard, Rev -4, Date: Monday, February 28, 2005

All place within 2" to CPU



1.8V is for Dothan A2 before.

1D5V OR 1D5V Intel suggest Dothan A2 or later only use 1.5V



Layout Note:  
VCCSENSE and VSSSENSE lines should be of equal length.

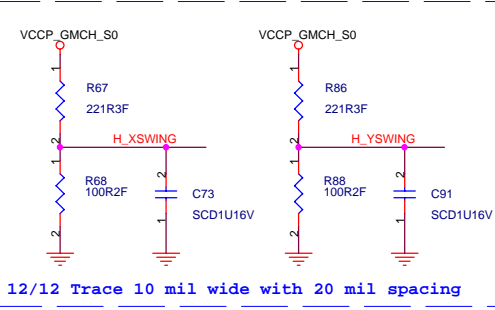
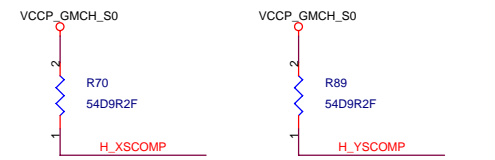
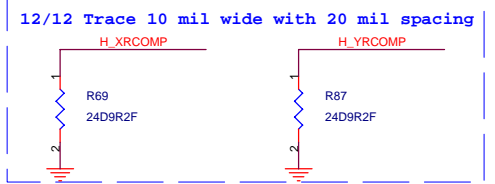
Layout Note:  
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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Title: CPU (2 of 2)

Size: A3 Document Number: Leopard Rev: -4

Date: Monday, February 28, 2005 Sheet: 5 of 41

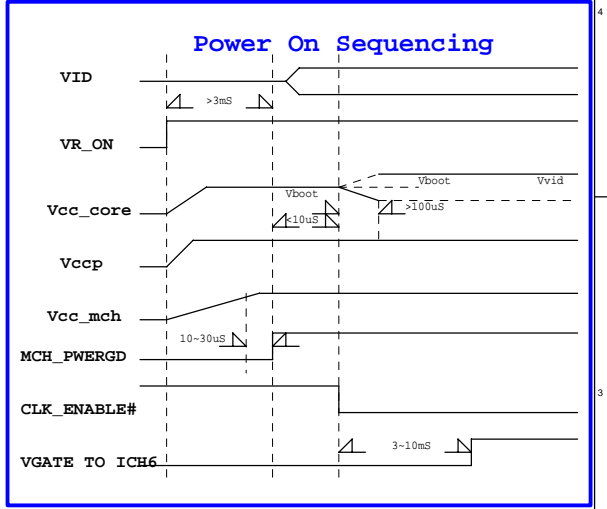
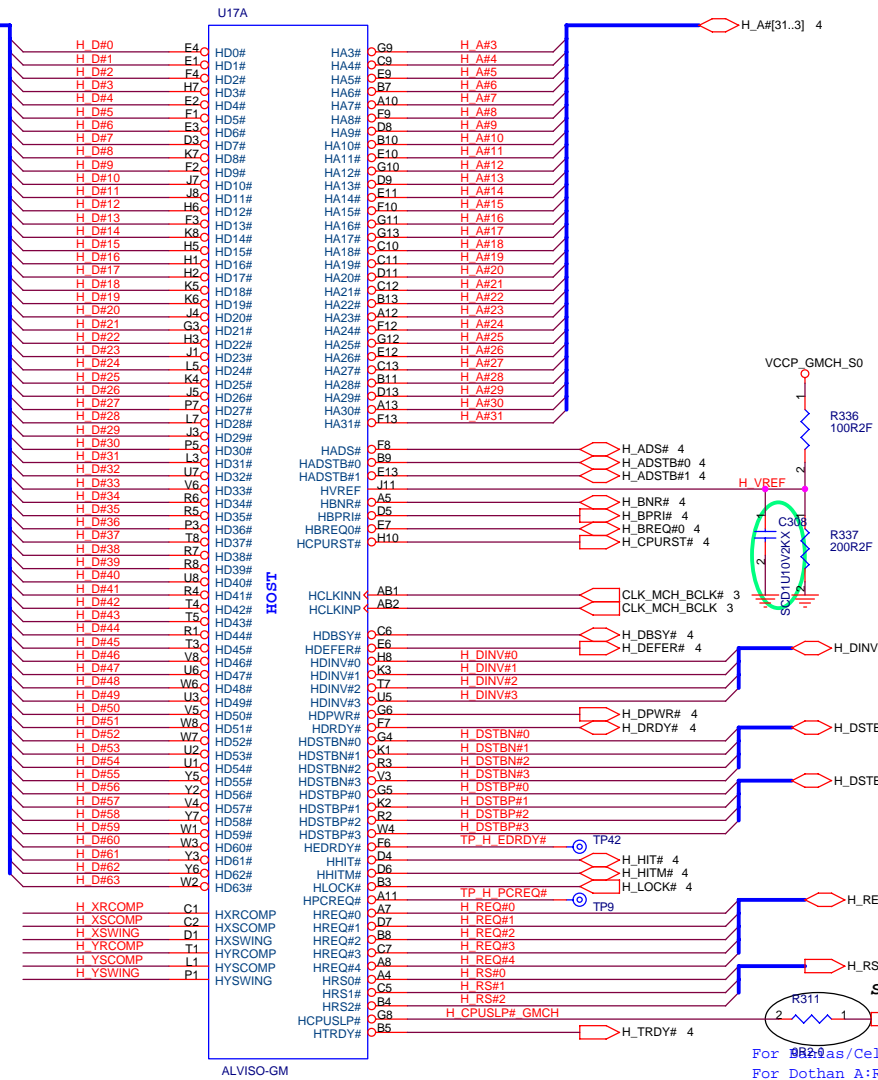


### Alviso Strapping Signals and Configuration

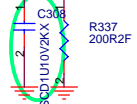
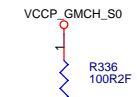
REV.NO. 1.0  
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = DDR1 (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present(Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.



2/10 HMI-SC  
Intel Sightings  
issue 54489



SC 0630  
For Dothan A:R93=DUMMY  
For Dothan B:R93=0R

ALVISO-GM: 71.0GMCH.08U  
ALVISO-PM: 71.0GMCH.0BU  
ALVISO-GML: 71.0GMCH.0JU

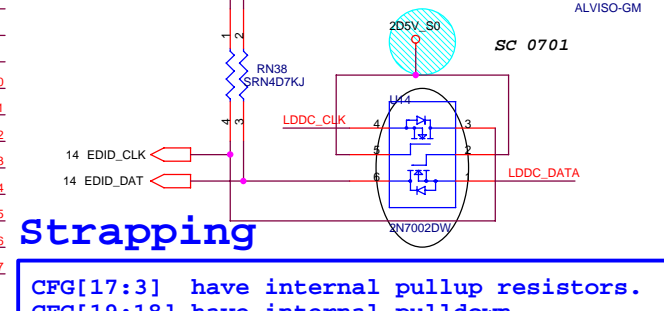
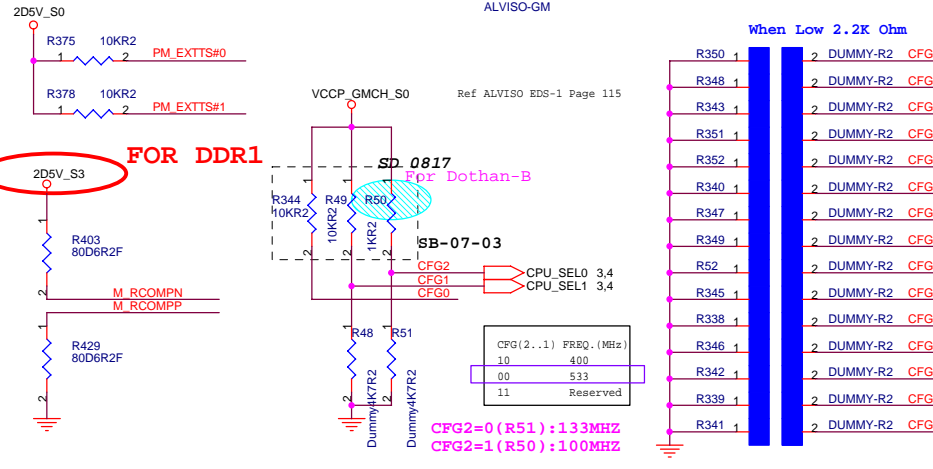
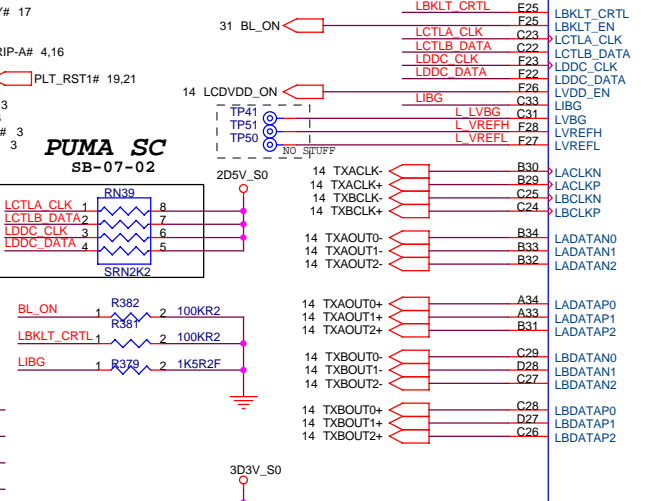
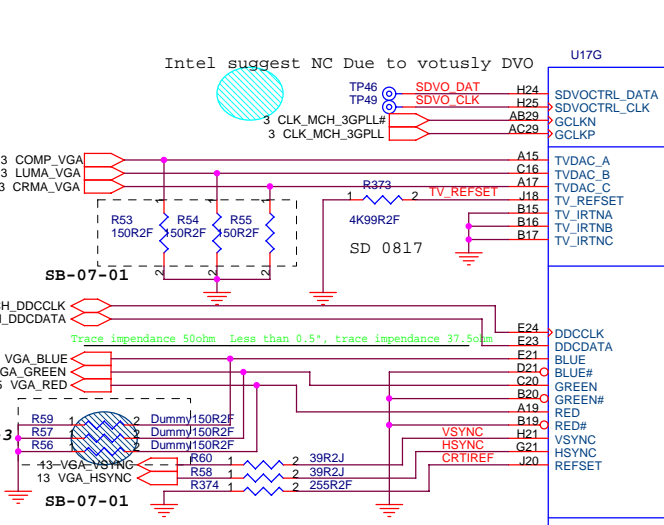
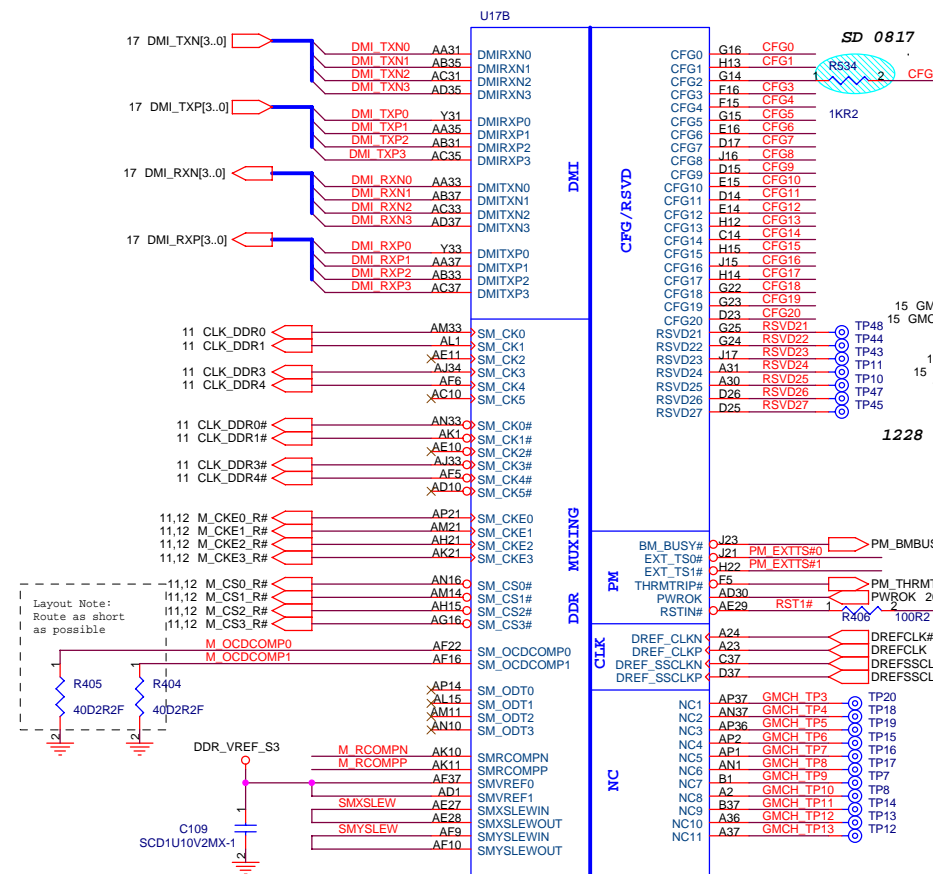
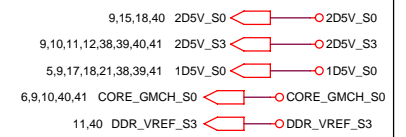
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Title: GMCH (1 of 5)

Size: A3 Document Number: Leopard Rev: -4

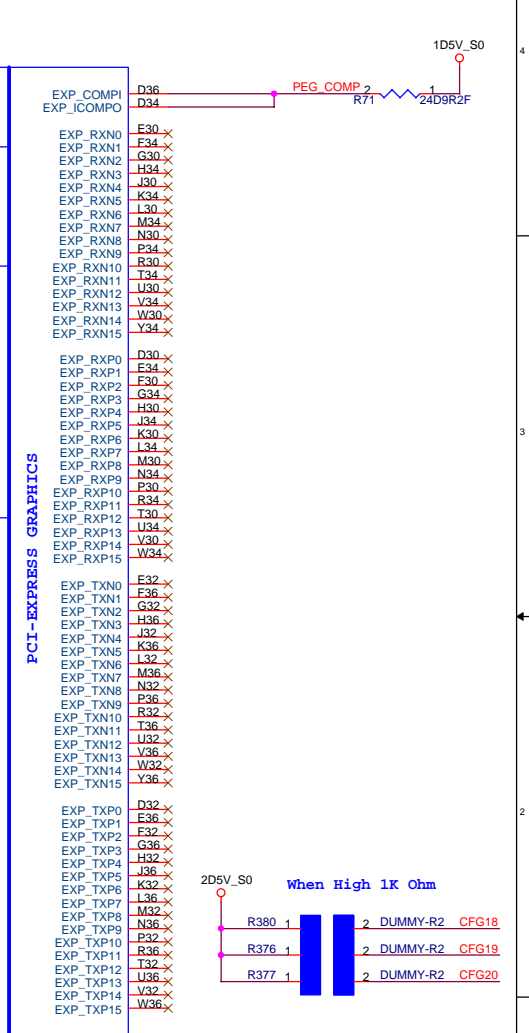
Date: Monday, February 28, 2005 Sheet: 6 of 41

Alviso will provide SDVO\_CTRLCLK and CTRLDATA pulldowns on-die



### Strapping

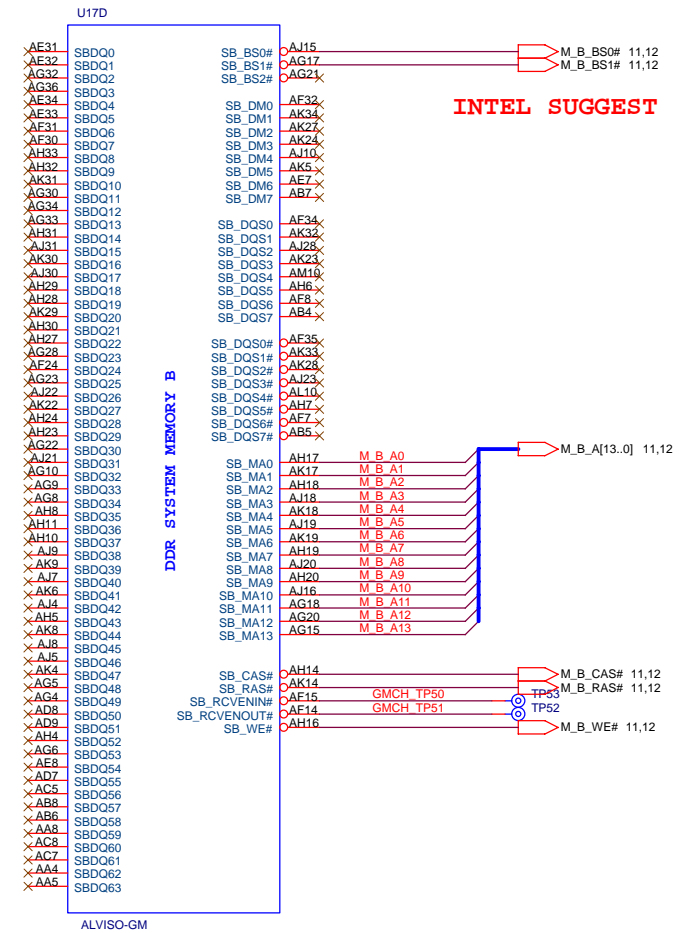
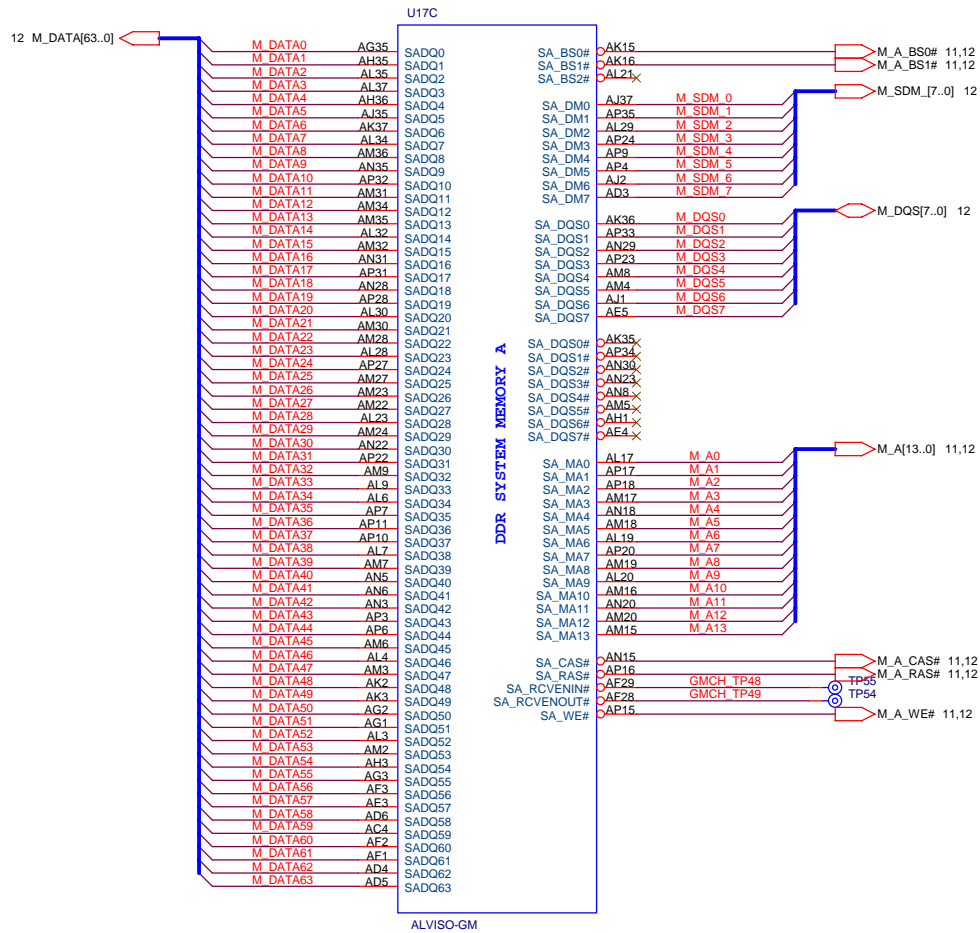
CFG[17:3] have internal pullup resistors.  
CFG[19:18] have internal pulldown resistors



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Title: GMCH (2 of 5)		
Size: A3	Document Number: Leopard	Rev: -4
Date: Monday, February 28, 2005 Sheet 7 of 41		

# SUPPORT DDR333 ONLY



**INTEL SUGGEST**

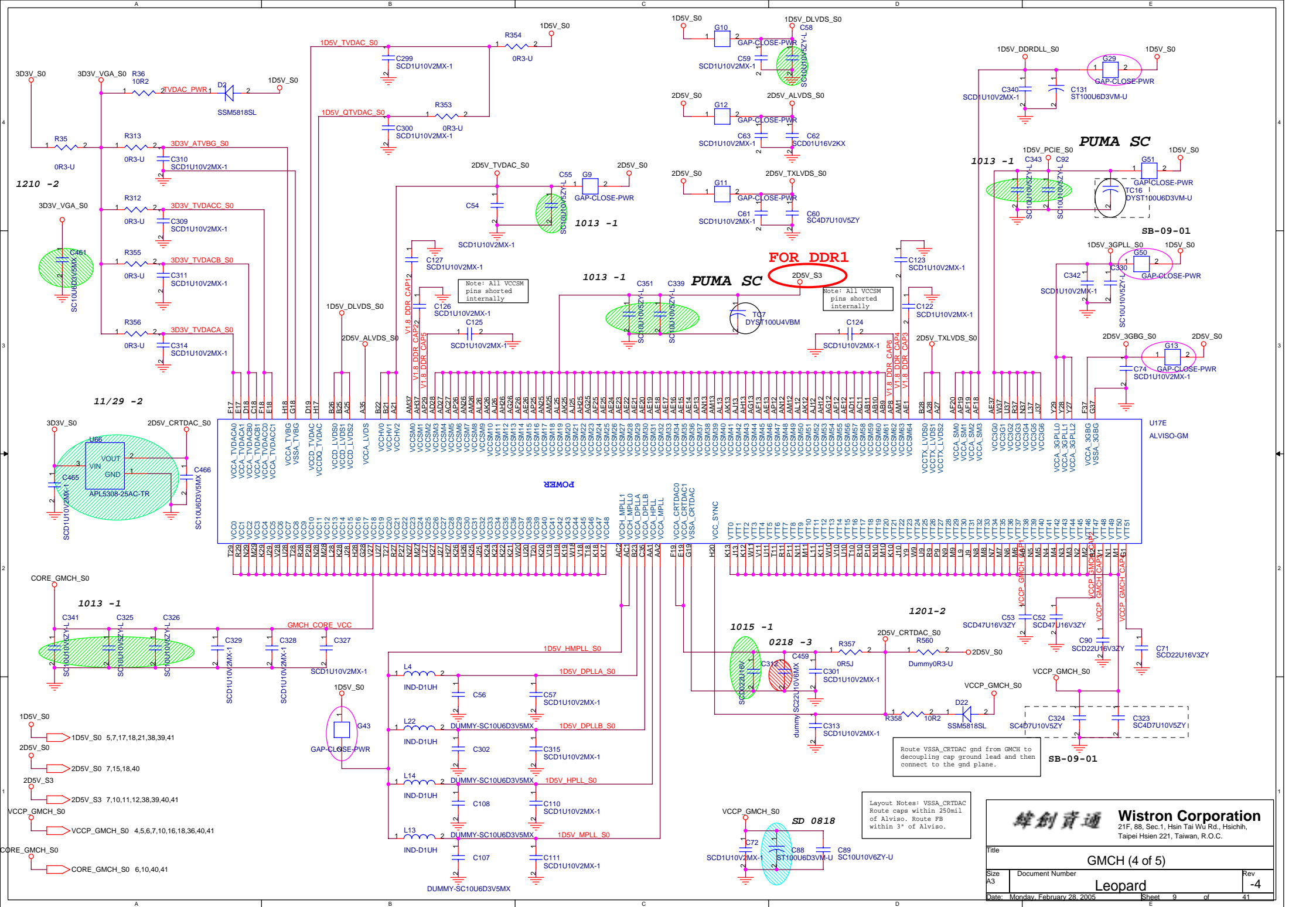
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Title: GMCH (3 of 5)

Size: A3 Document Number: Leopard Rev: -4

Date: Monday, February 28, 2005 Sheet: 8 of 41



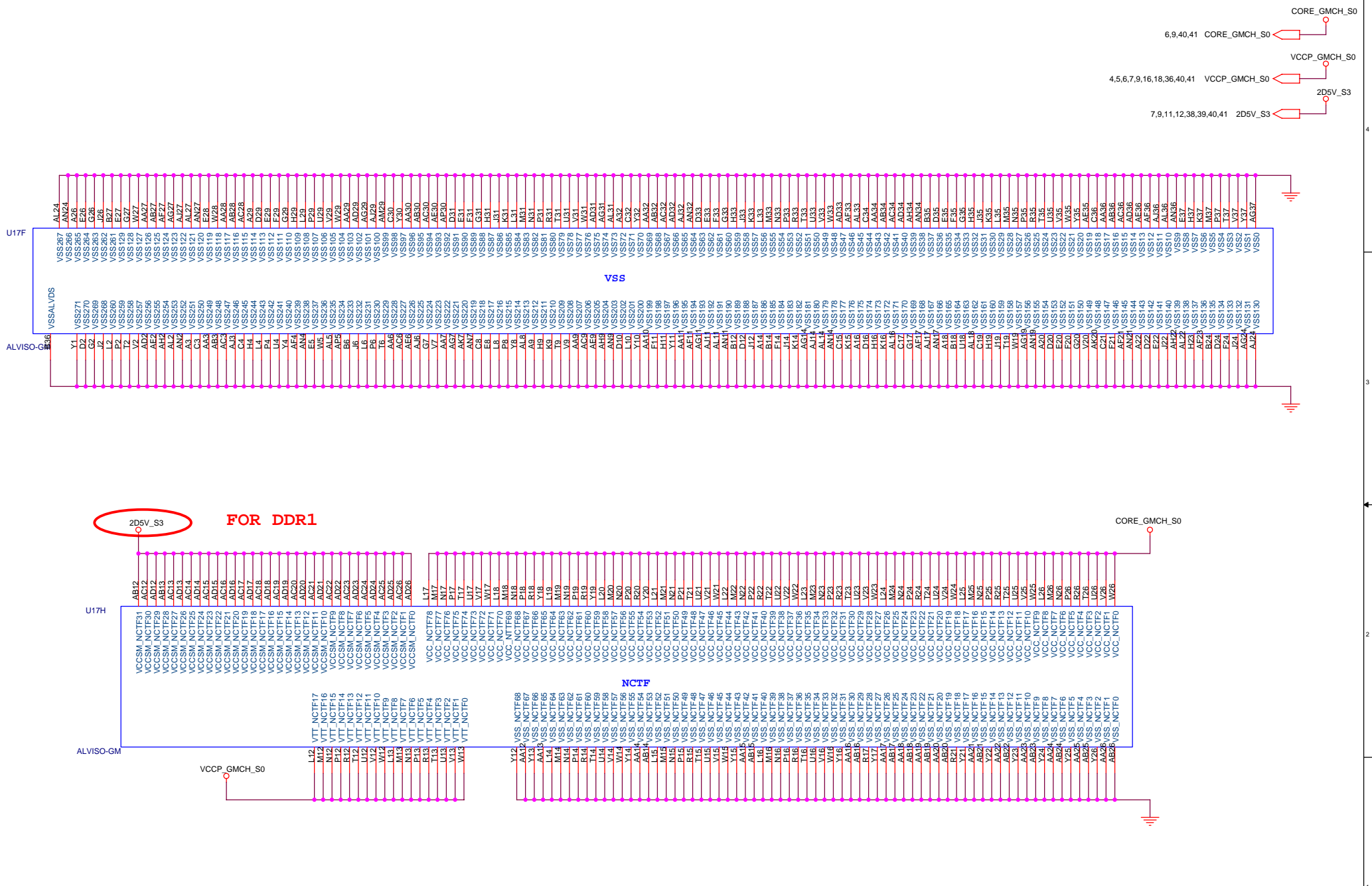


Route VSSA\_CRTDACC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Layout Notes: VSSA\_CRTDACC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

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Title <b>GMCH (4 of 5)</b>		
Size A3	Document Number <b>Leopard</b>	Rev -4
Date: Monday, February 28, 2005      Sheet 9 of 41		

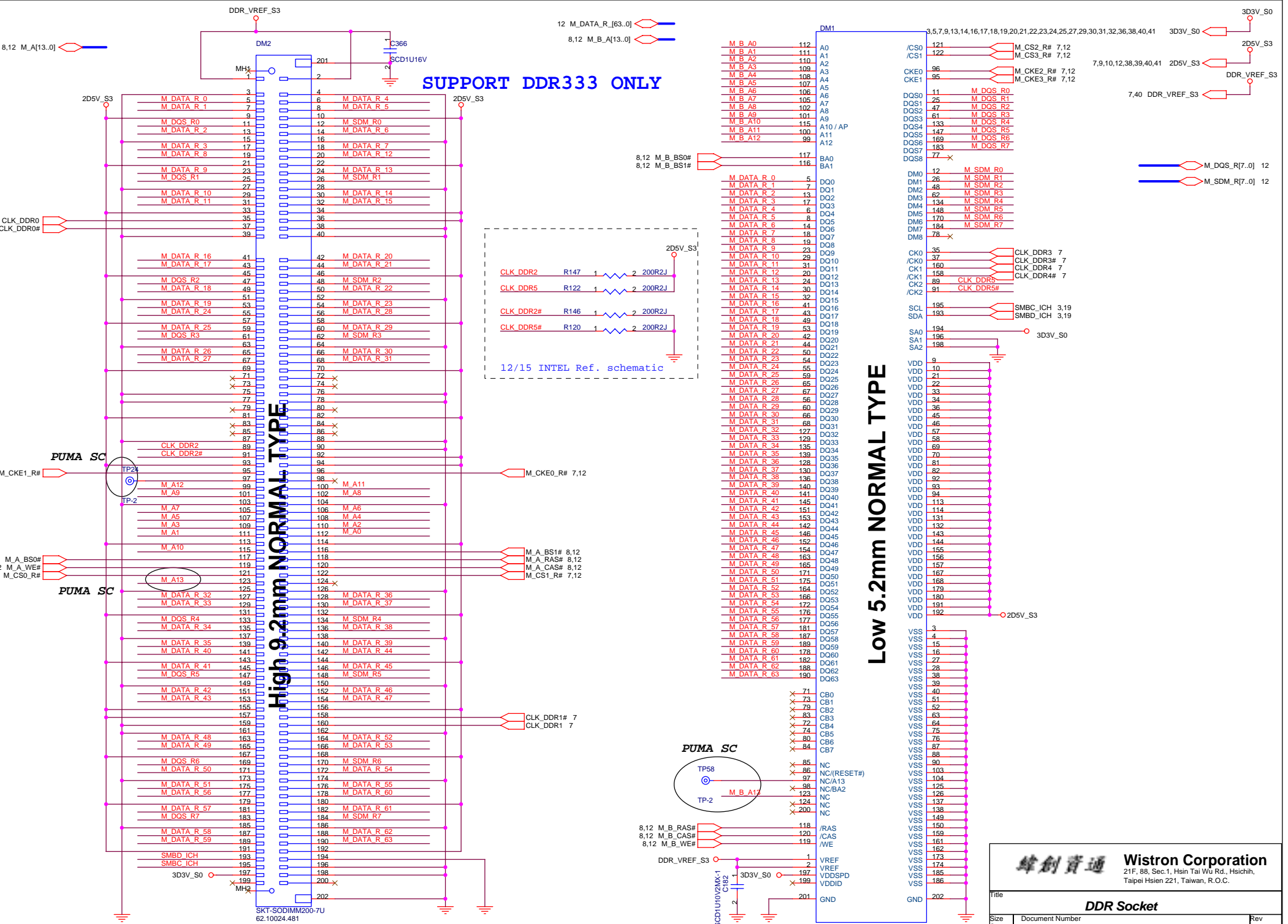


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Title: GMCH (5 of 5)

Size: A3 | Document Number: Leopard | Rev: -4

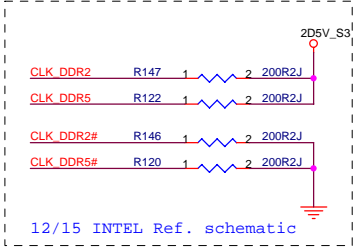
Date: Monday, February 28, 2005 | Sheet: 10 of 41



**SUPPORT DDR333 ONLY**

**High 9.2mm NORMAL TYPE**

**Low 5.2mm NORMAL TYPE**

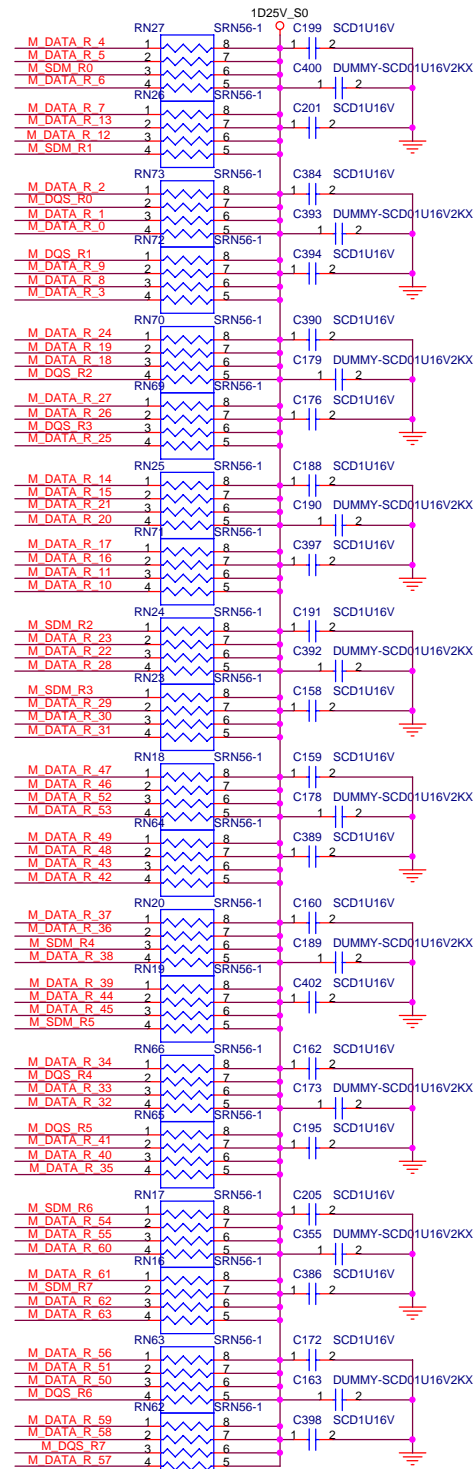
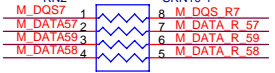
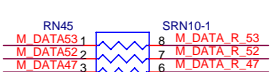
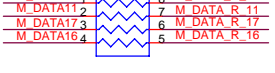
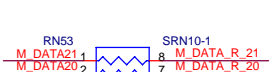
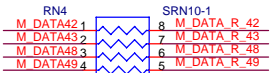
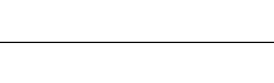
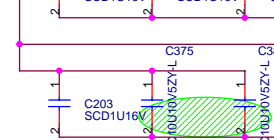
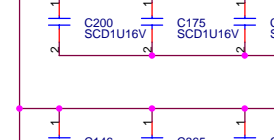
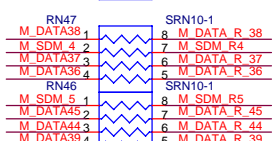
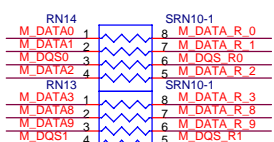
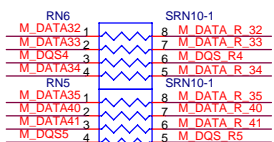
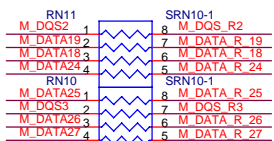
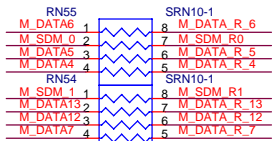
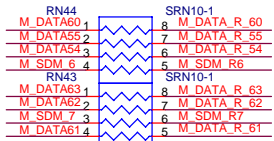


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<b>DDR Socket</b>	
Title	Document Number
Size	Rev
Custom	<b>Leopard</b>
Date: Monday, February 28, 2005	Sheet 11 of 41

# SERIES DAMPING

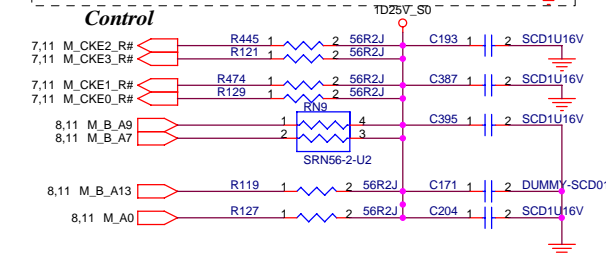
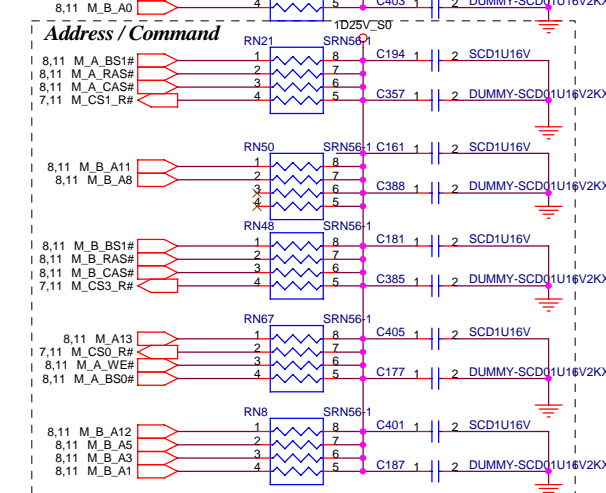
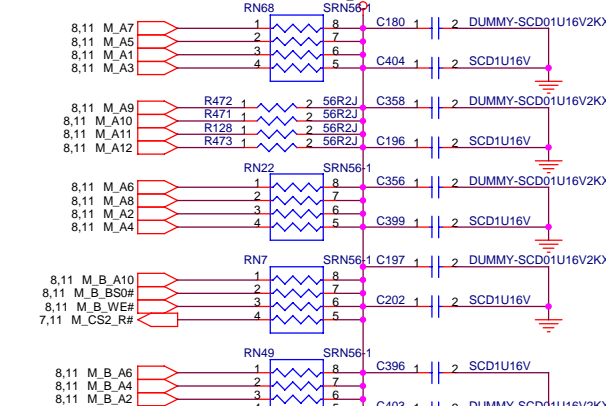
## PUMA-SC

Change RN to small size



# PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2  
NO EQUAL LENGTH LIMITATION

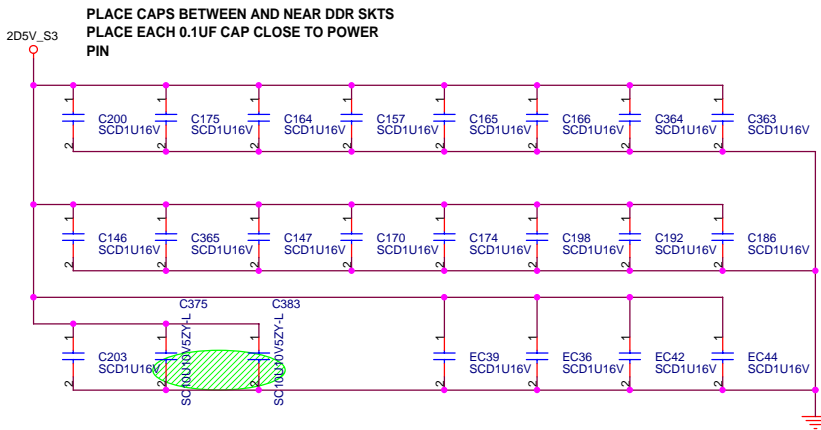


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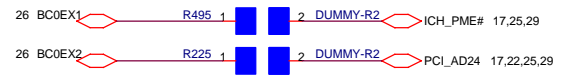
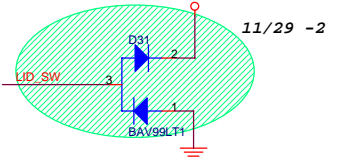
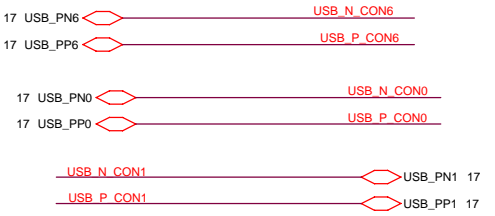
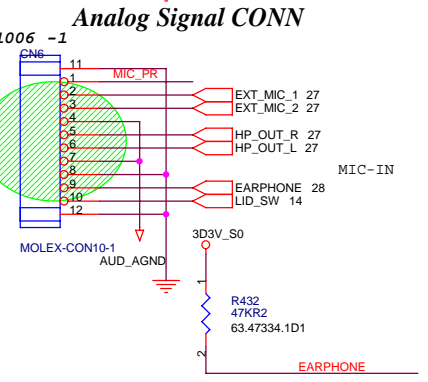
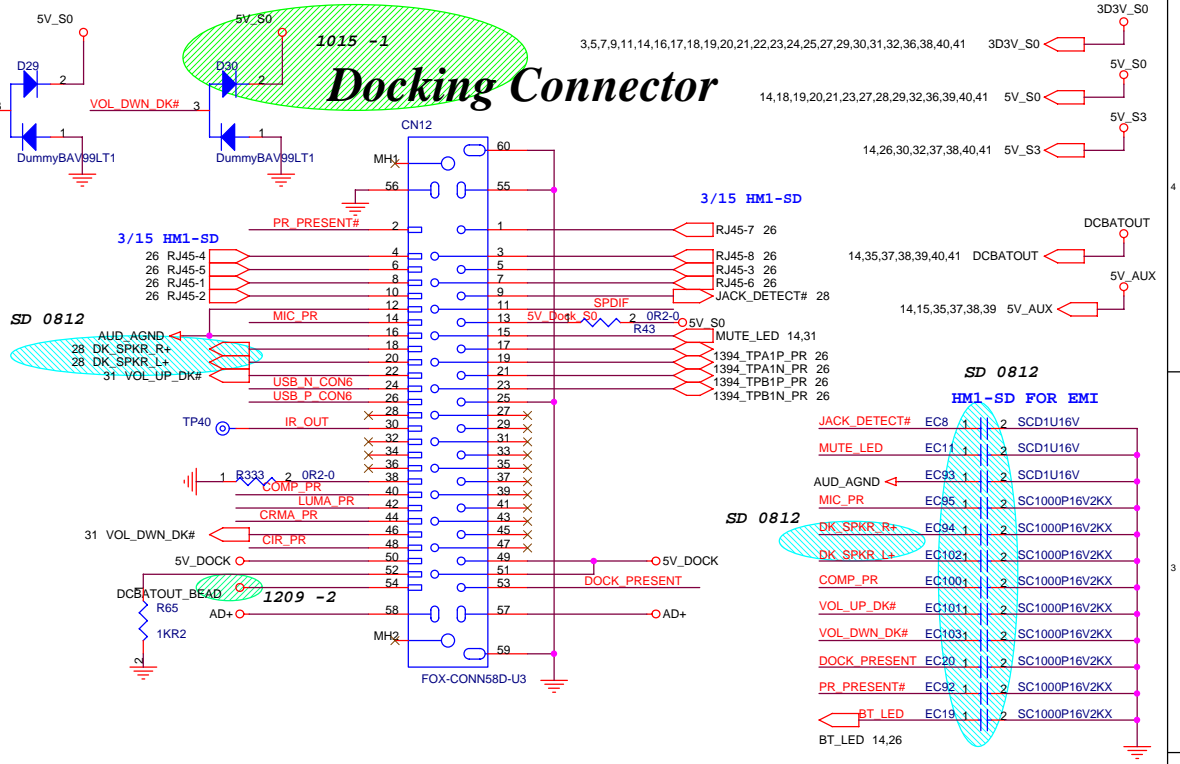
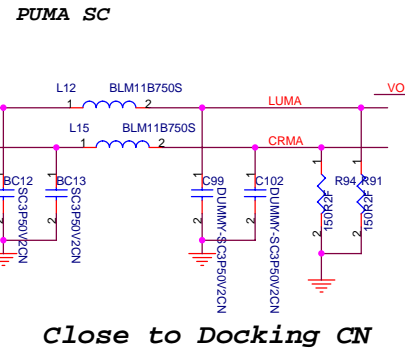
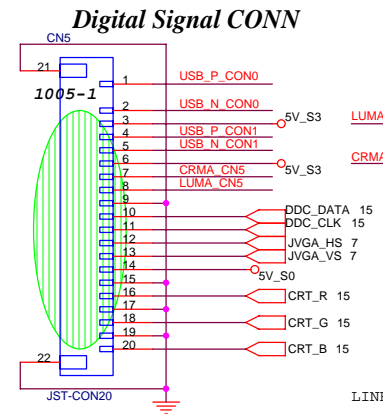
Title: **DDR Serial/Terminator Resistor**

Size: A3 | Document Number: **Leopard** | Rev: **-4**

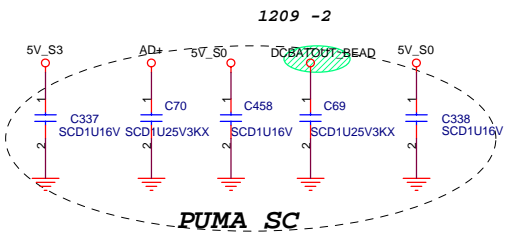
Date: Monday, February 28, 2005 | Sheet: 12 of 41



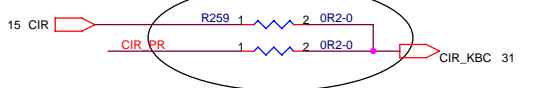
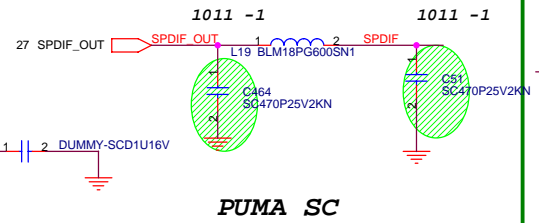
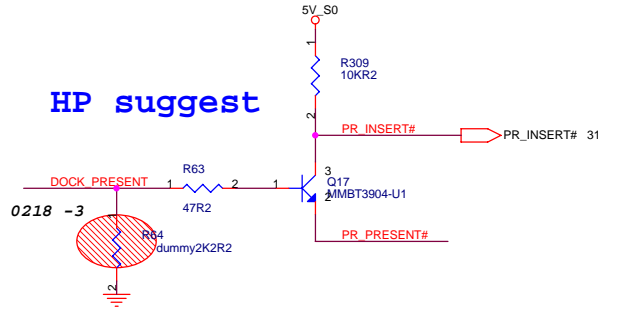
PLACE CAPS BETWEEN AND NEAR DDR SKTS  
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN



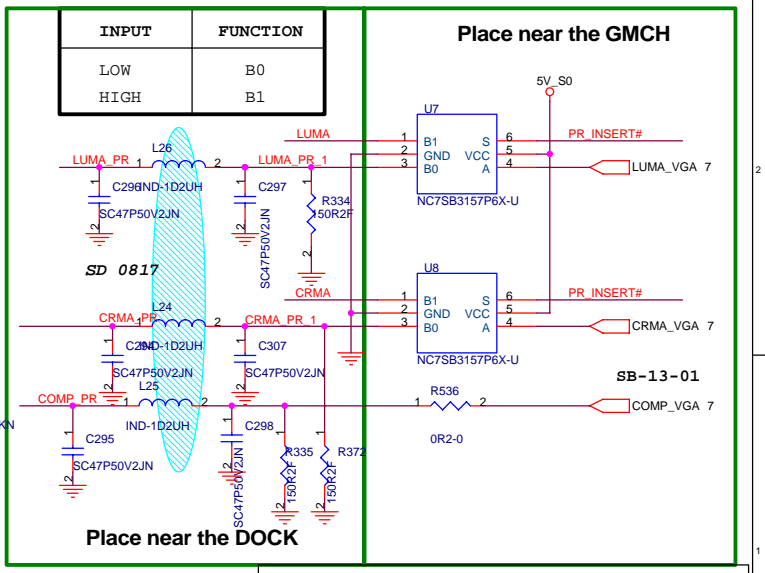
Please close to ICH6



HP suggest

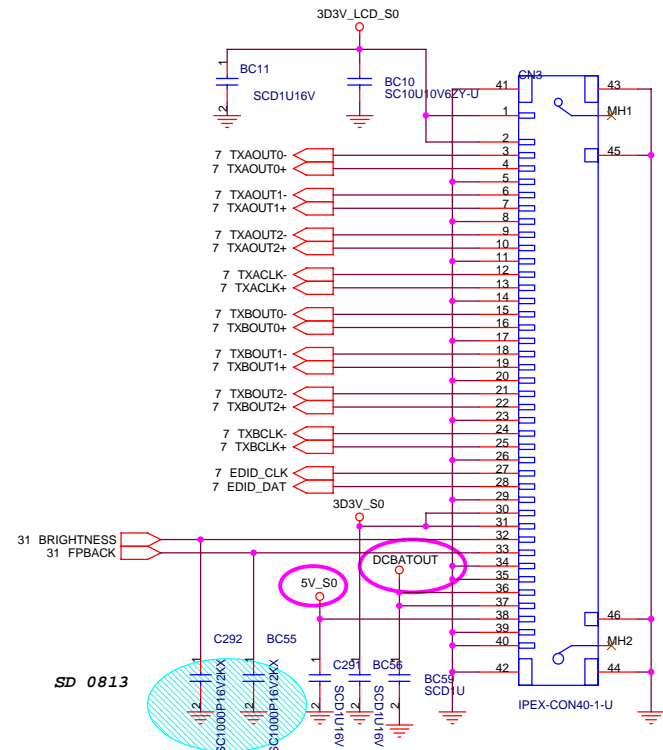


CIR, CIR\_PR, CIR\_KBC are connect together. default setting 12/12



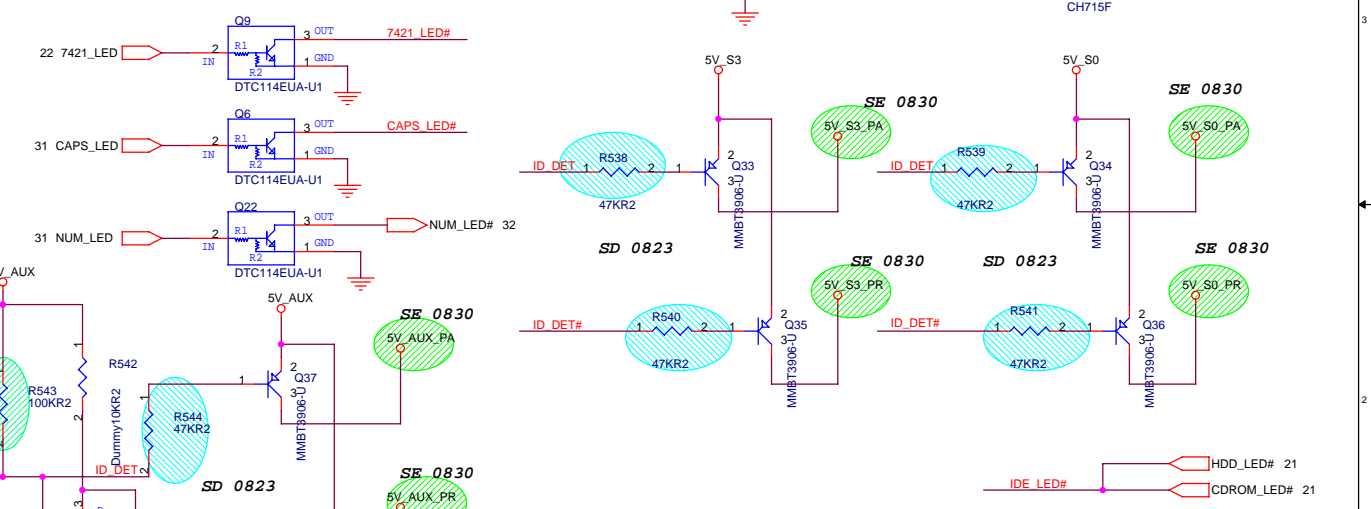
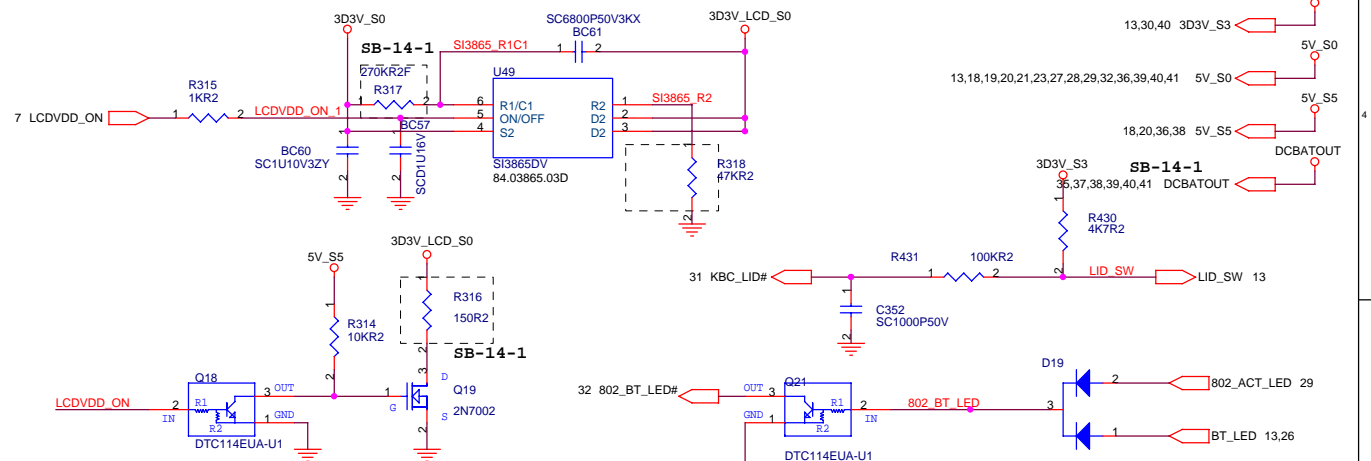
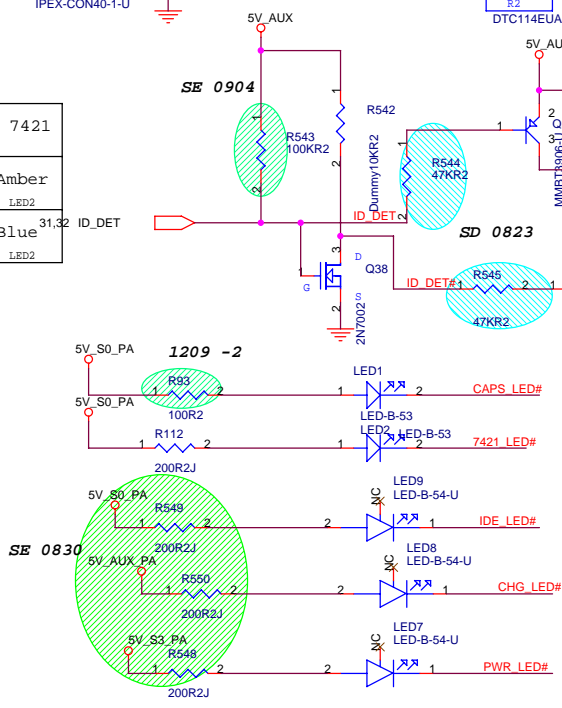
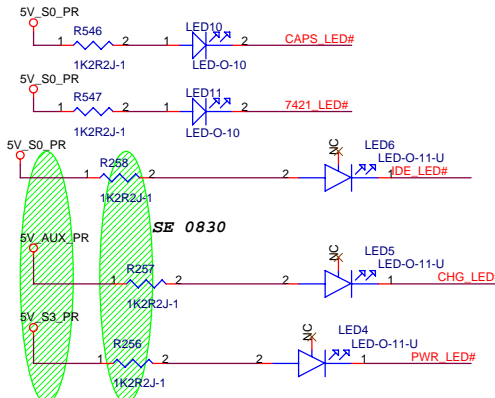
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# INVERTER/LCD



	PWR	CHR	HDD	IR	CAPS	7421
PR Botton	Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top	Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

SC 0705  
change R from 100 to 200 ohm  
**PUMA SC**



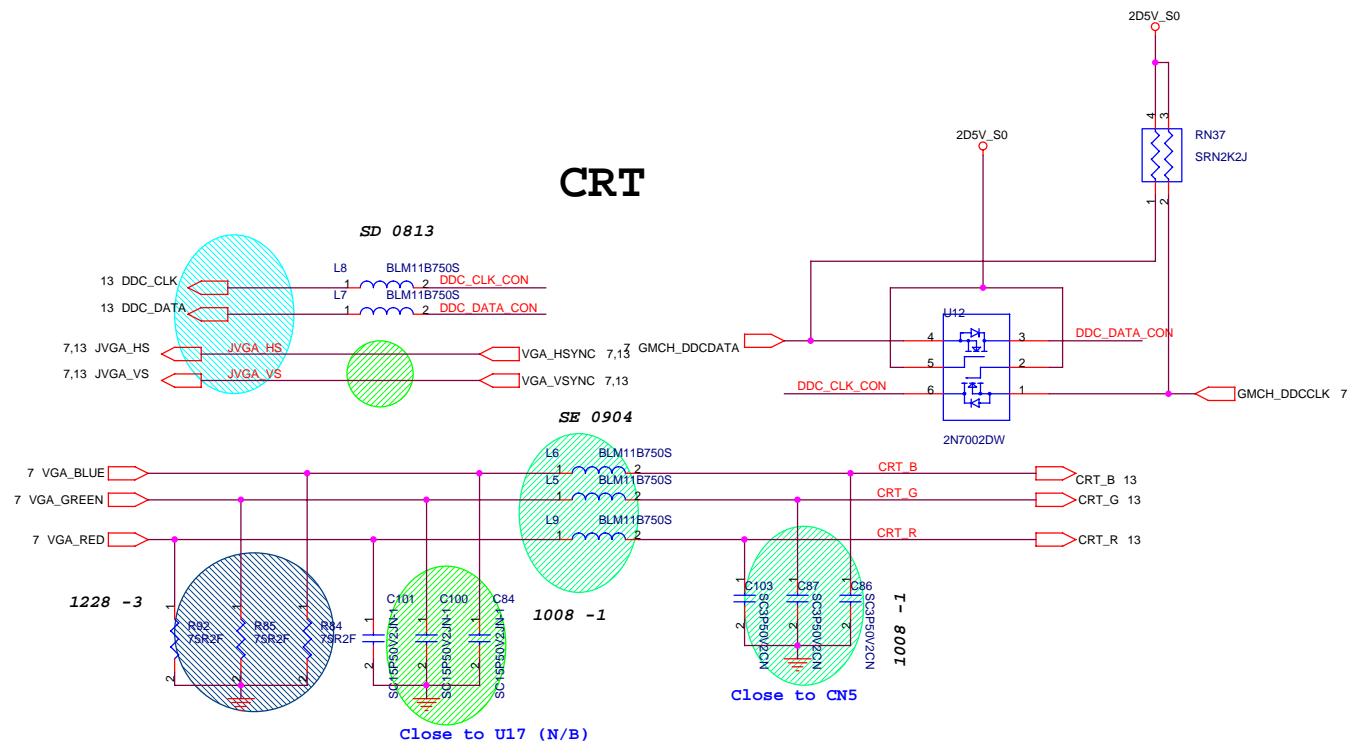
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Title <b>Inverter/LCD</b>		
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PA & PR diffent parts

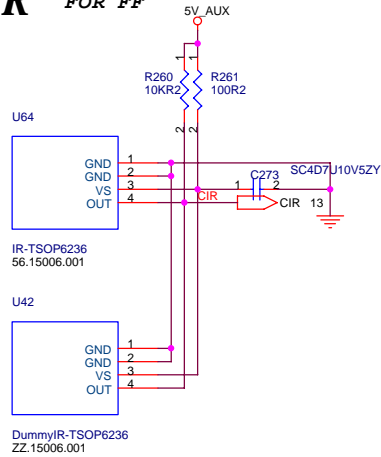
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1

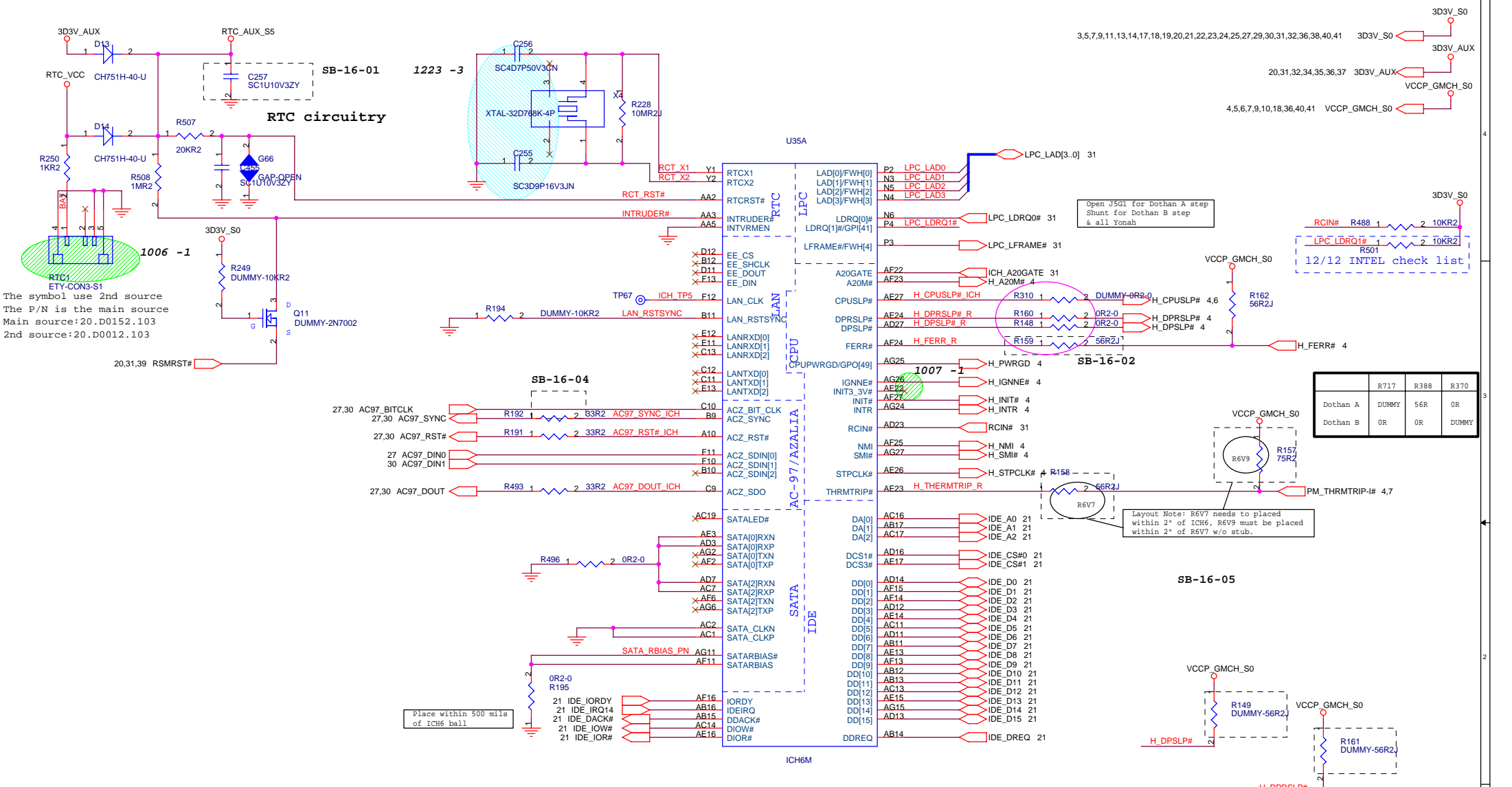
CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1



010804 Modified on Astro ID request

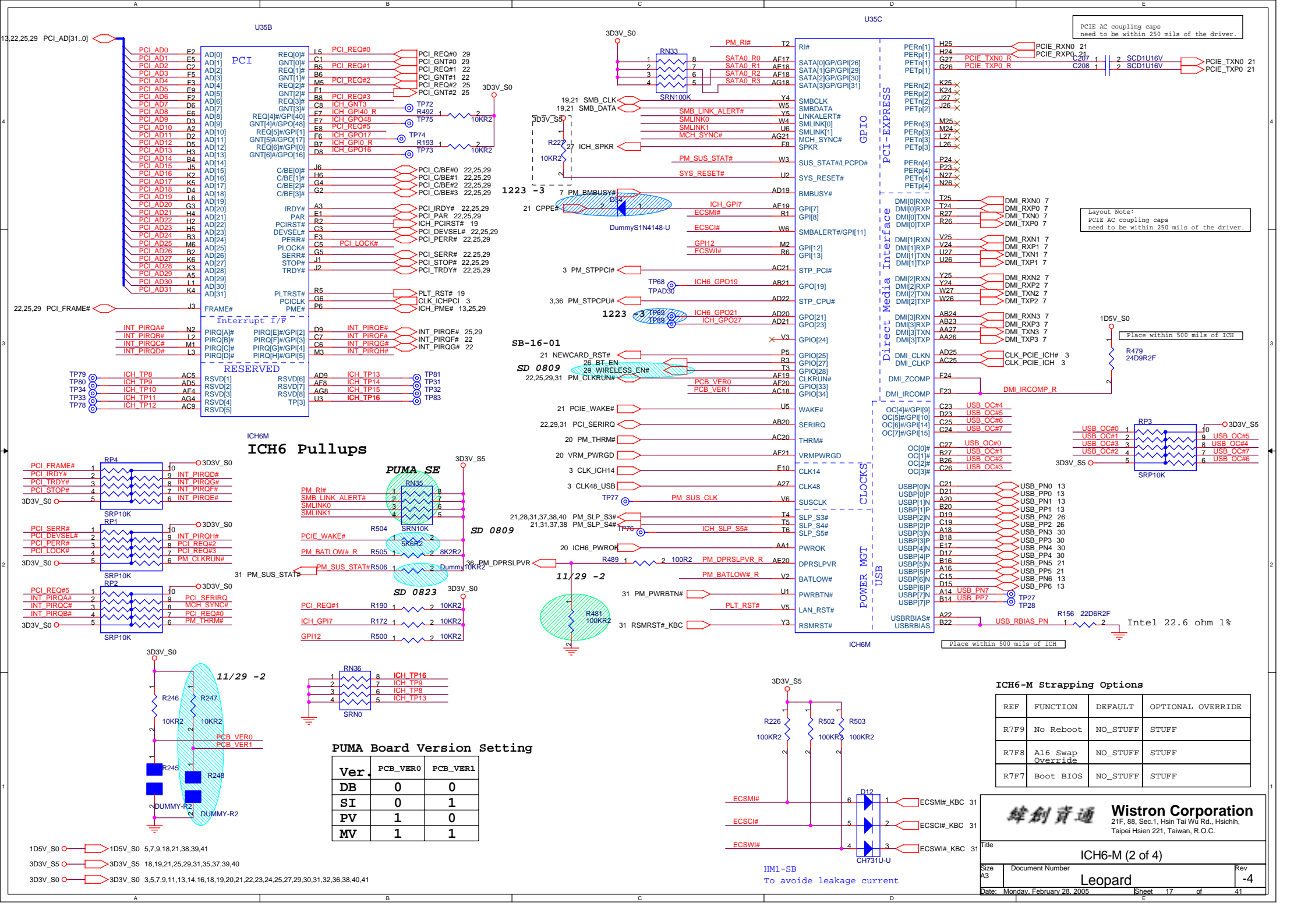
**CIR FOR FF**





	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY





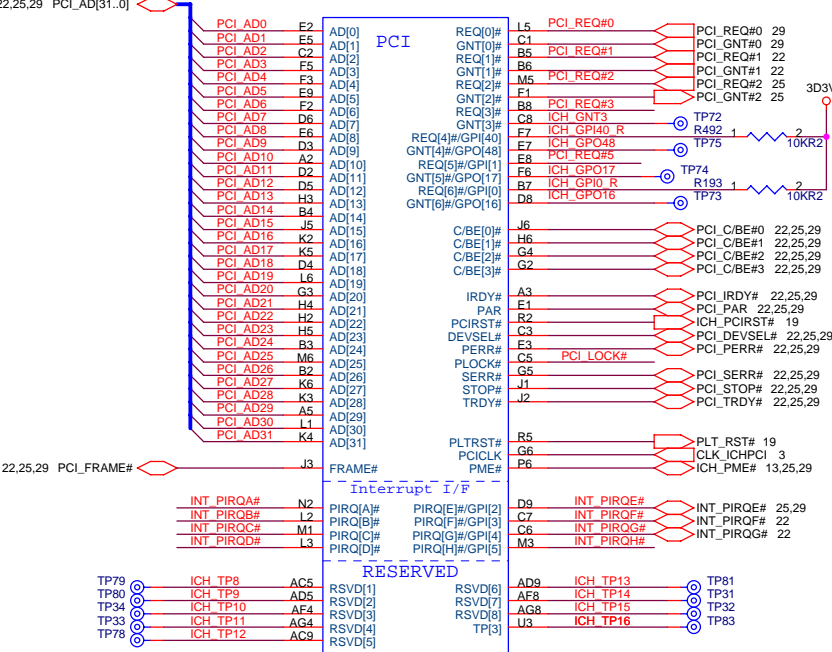
PCIe AC coupling caps need to be within 250 mils of the driver.

Layout Note: PCIe AC coupling caps need to be within 250 mils of the driver.

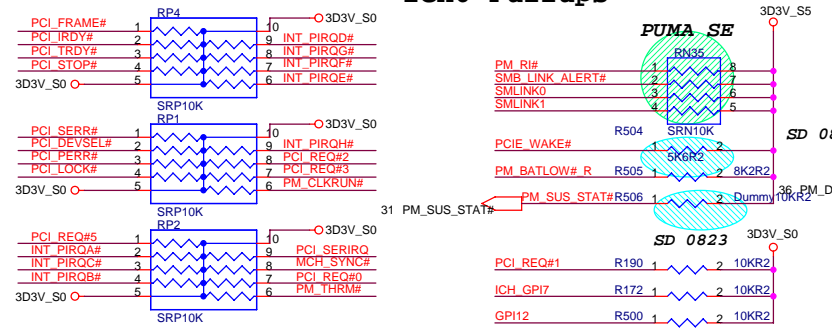
Place within 500 mils of ICH

Place within 500 mils of ICH

### U35B



### ICH6M ICH6 Pullups



### PUMA Board Version Setting

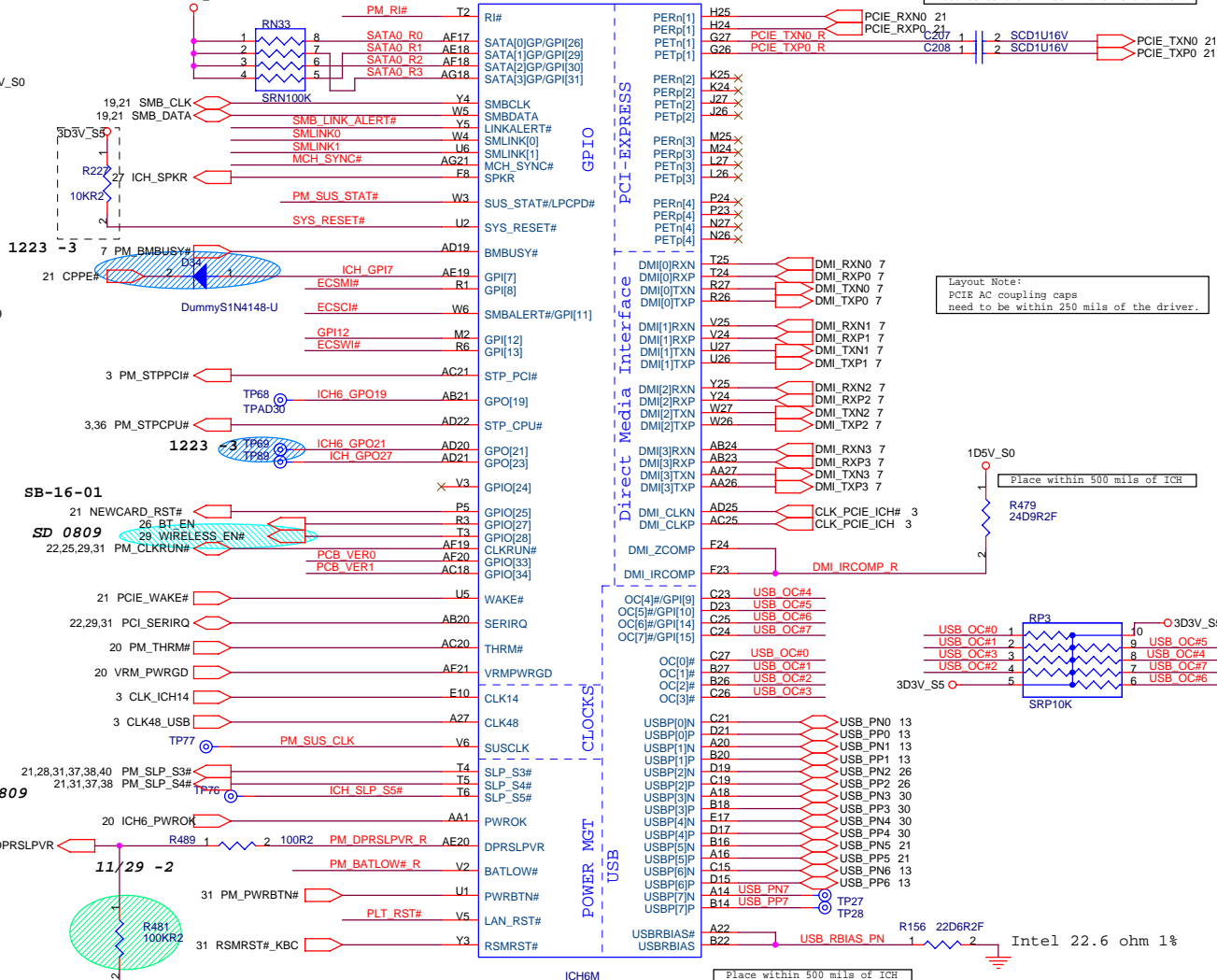
Ver.	PCB_VER0	PCB_VER1
DB	0	0
SI	0	1
PV	1	0
MV	1	1

### ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

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### U35C

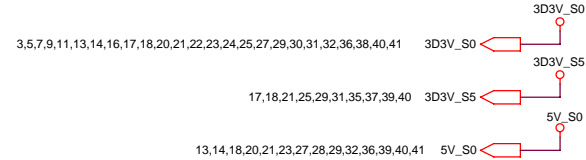
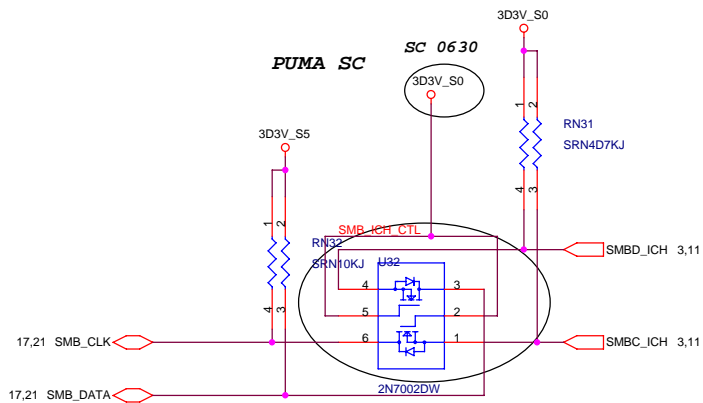


HM1-SB  
To avoid leakage current

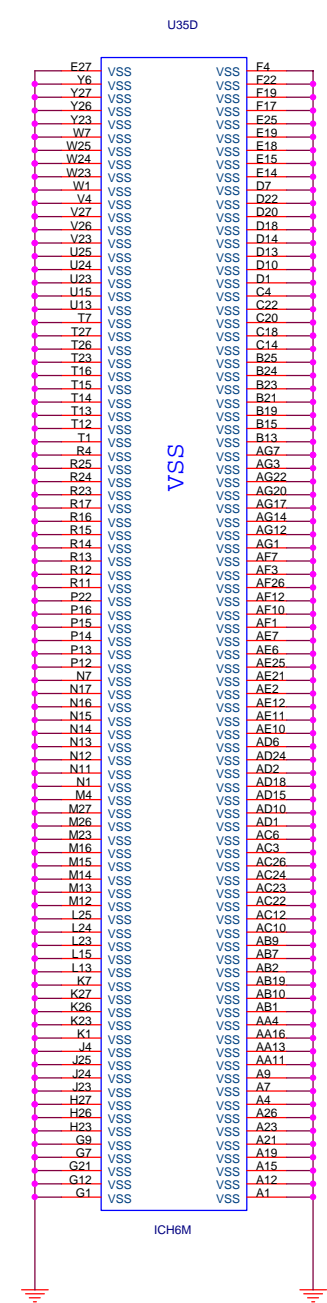
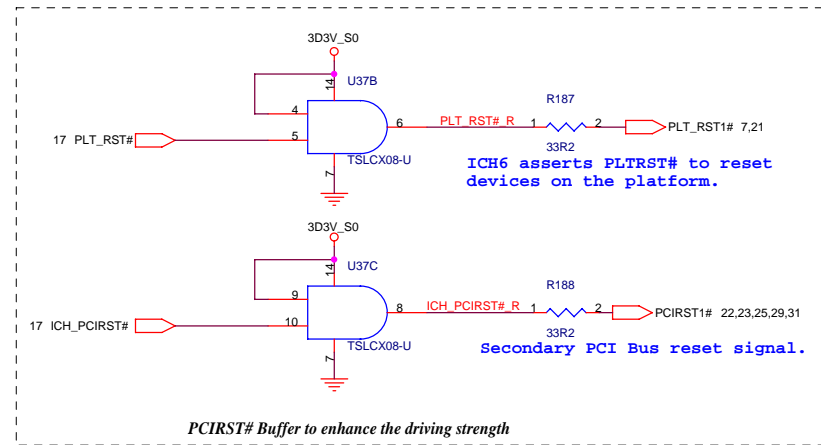
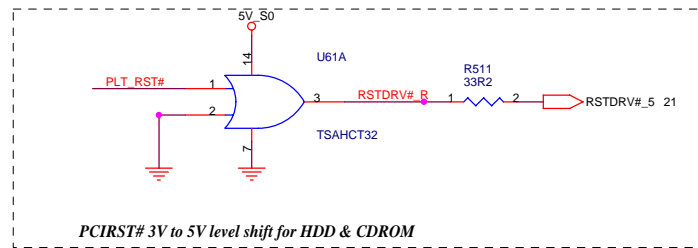
1D5V\_S0 → 1D5V\_S0 5,7,9,18,21,38,39,41  
 3D3V\_S5 → 3D3V\_S5 18,19,21,25,29,31,35,37,39,40  
 3D3V\_S0 → 3D3V\_S0 3,5,7,9,11,13,14,16,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41



**SMBUS (ICH6 ----> SODIMM,CLKGEN)**



**PUMA SC**

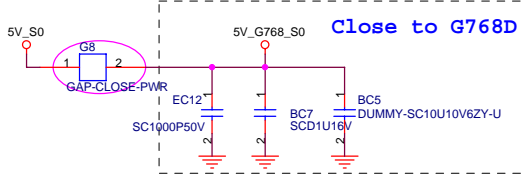


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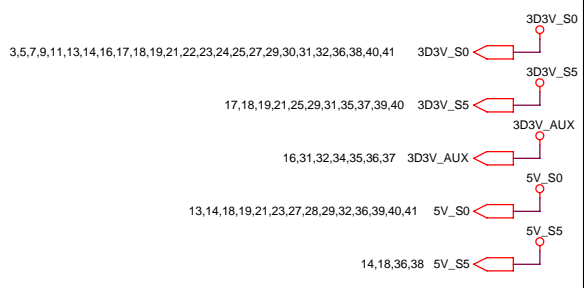
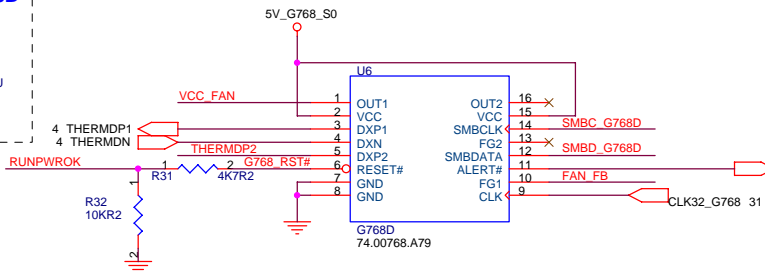
Title: ICH6-M (4 of 4)

Size A3    Document Number    Rev -4

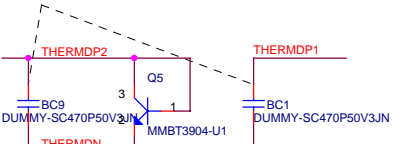
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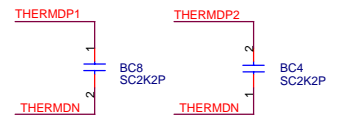
Reserve for G768B works at High Speed



Put these two Caps near the thermal diode.

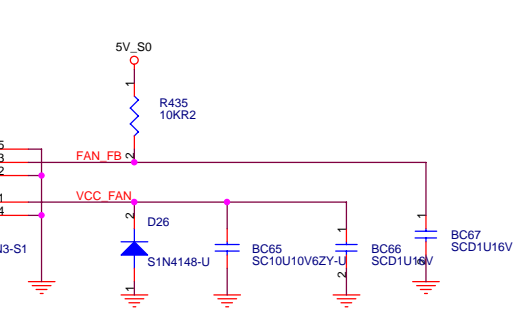


SYSTEM SENSOR

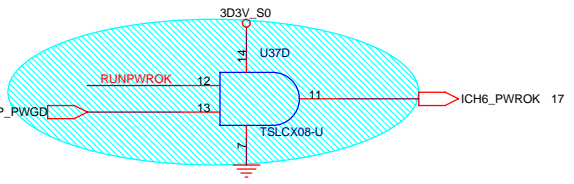
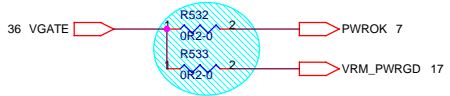
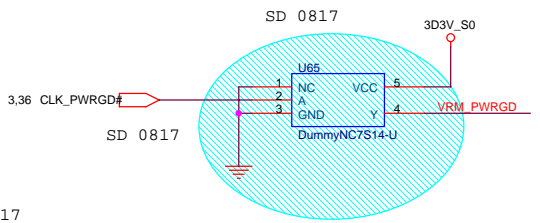


THERMDP1/DP2/THERMDN ON THE SAME LAYER  
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS  
CAPS CLOSE TO G768B

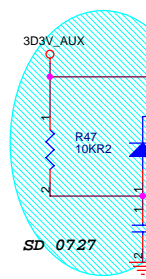
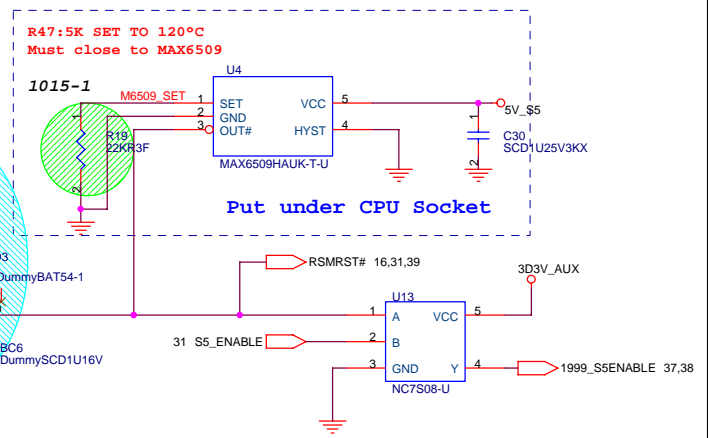
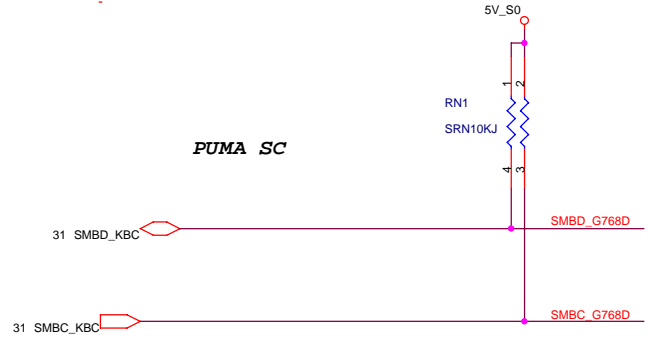
180 ms after VCC\_G768 > 4.38v, p2, 7



The symbol use 2nd source  
The P/N is the main source  
Main source:20.D0152.103  
2nd source:20.D0012.103

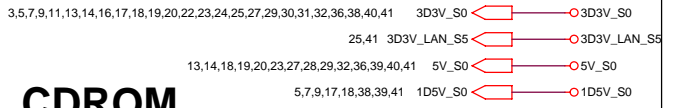
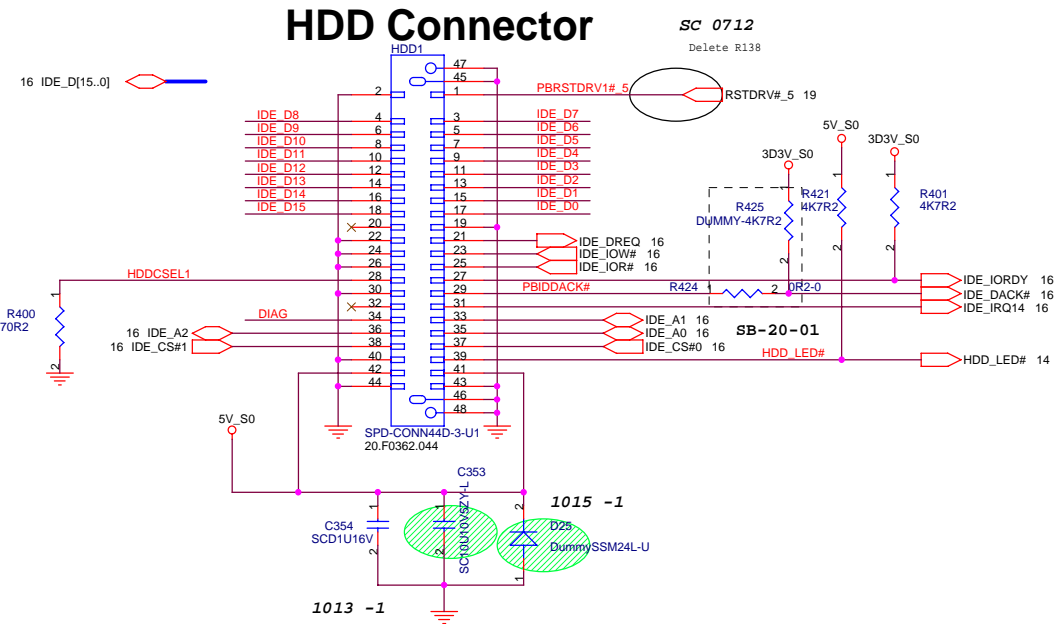


PUMA SC



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Title		
<b>G768D</b>		
Size	Document Number	Rev
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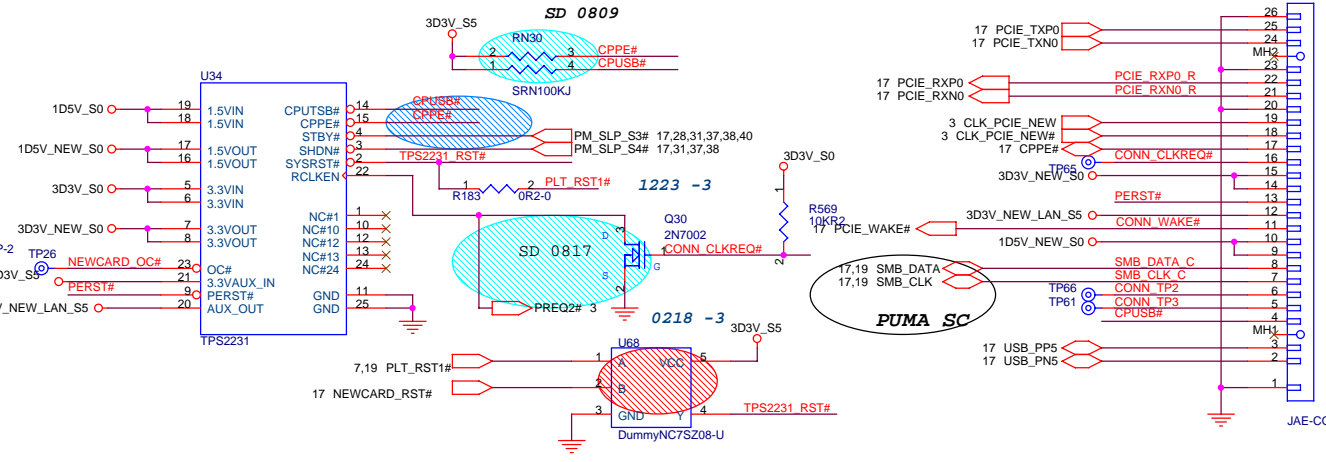
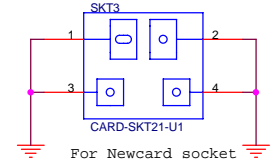
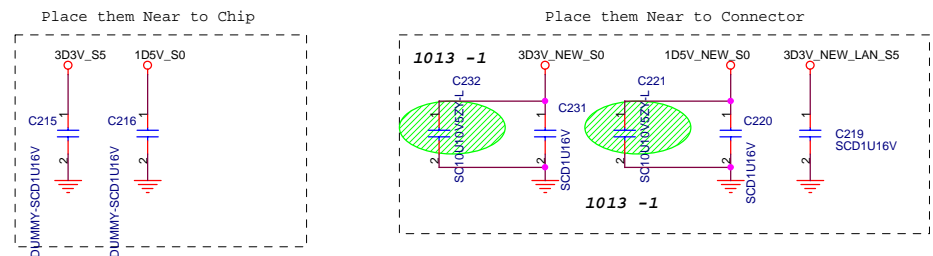
# HDD Connector



# CDROM

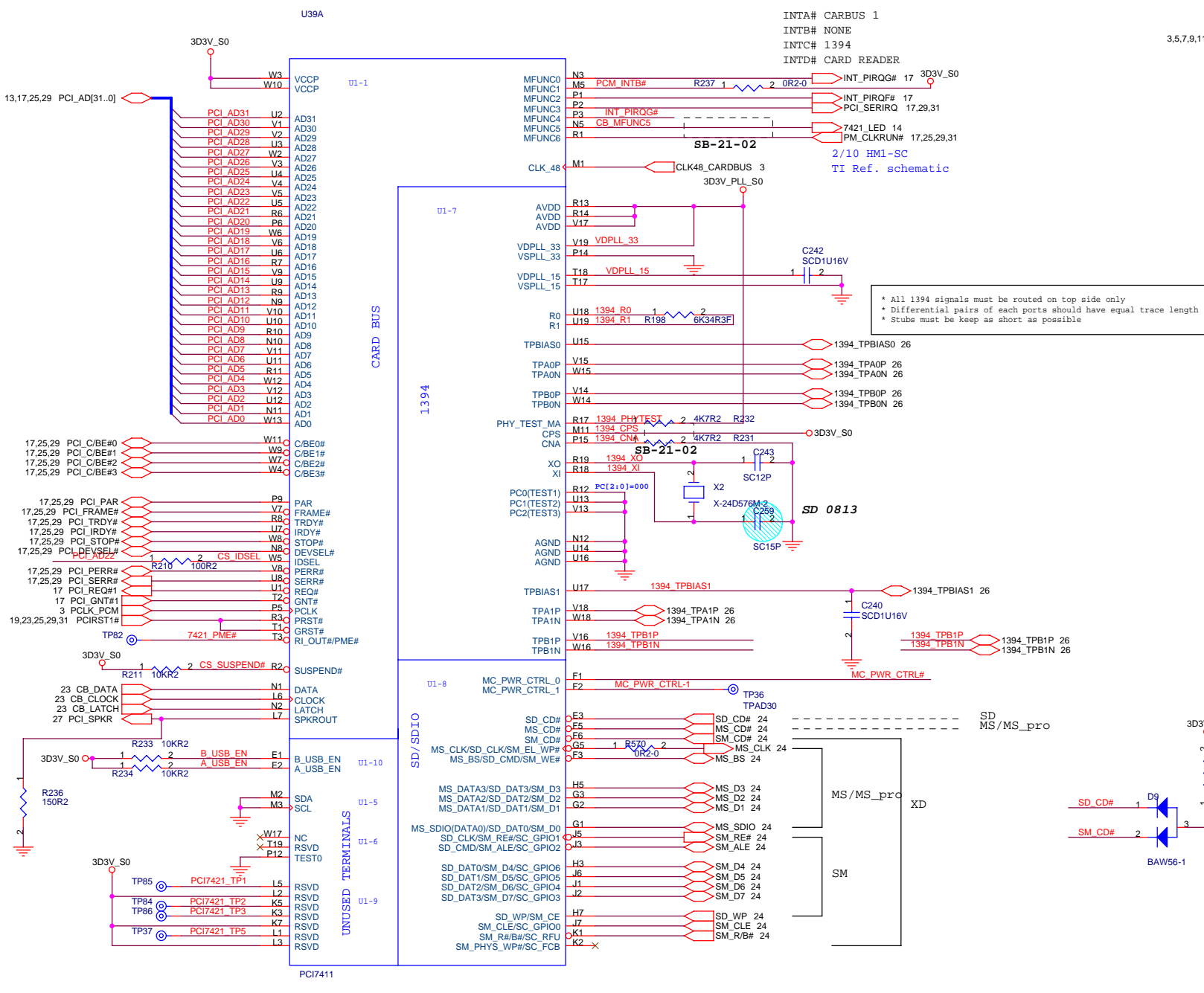
PIN 49,50 DON'T USE  
 The symbol use 2nd source  
 The P/N is the main source  
 Main source:20.10150.050  
 2nd source:20.B0040.050

# NEWCARD Connector



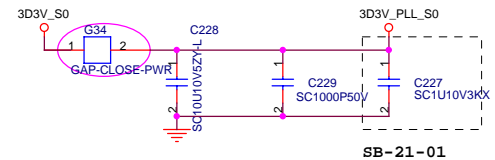
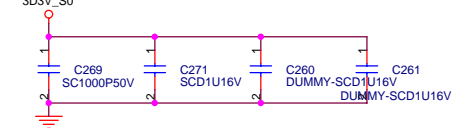
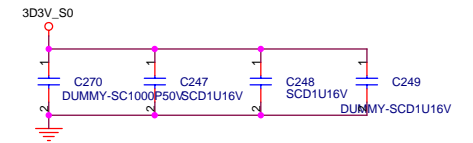
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>HDD / CDROM/NEWCARD</b>	
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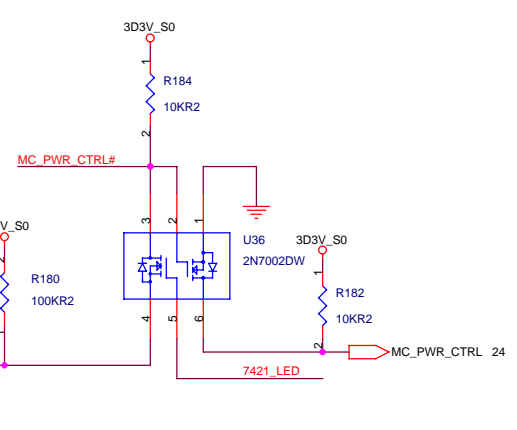


3.5,7,9,11,13,14,16,17,18,19,20,21,23,24,25,27,29,30,31,32,36,38,40,41 3D3V\_S0

Bypass/Decoupling Capacitors  
Should be placed as close to  
PCI7421 as possible



\* All 1394 signals must be routed on top side only  
\* Differential pairs of each ports should have equal trace length  
\* Stubs must be kept as short as possible



7411:71.07411.00U  
7421:71.07421.00U

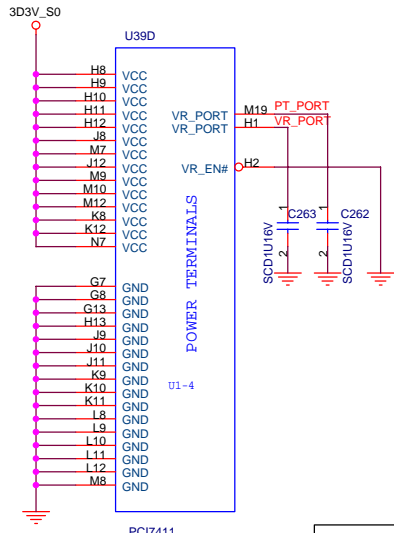
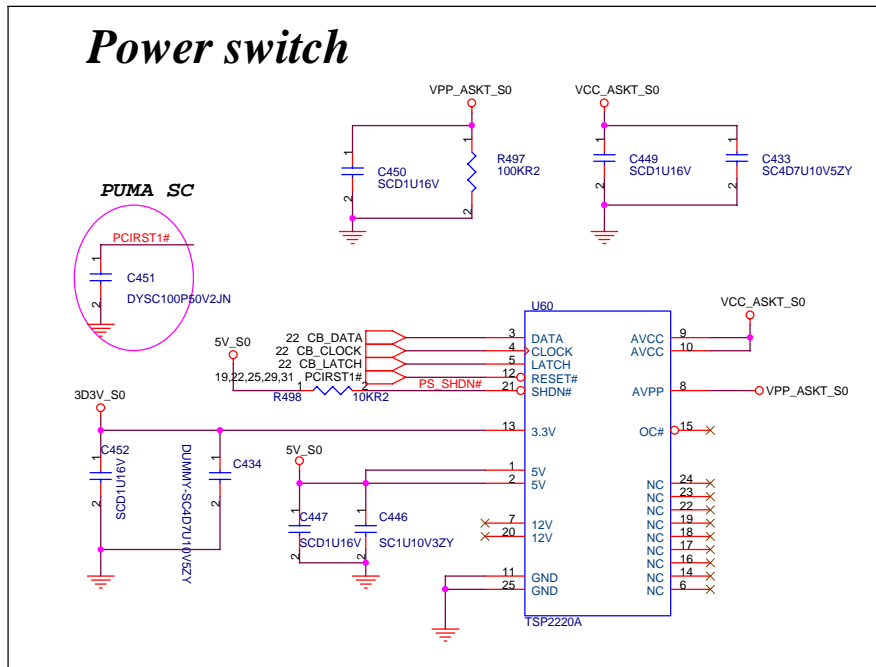
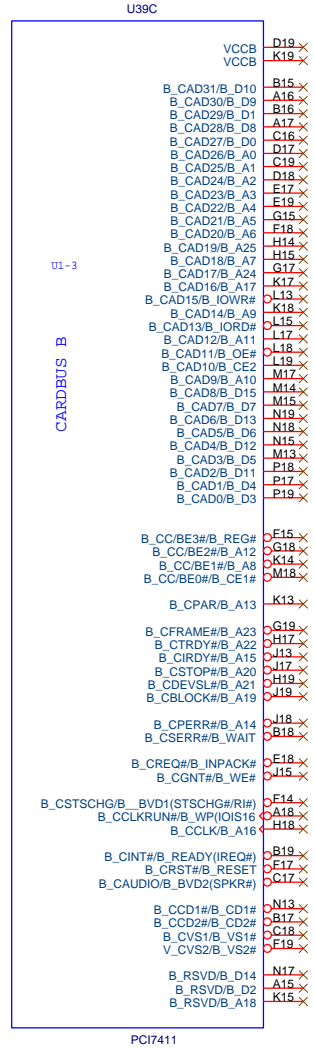
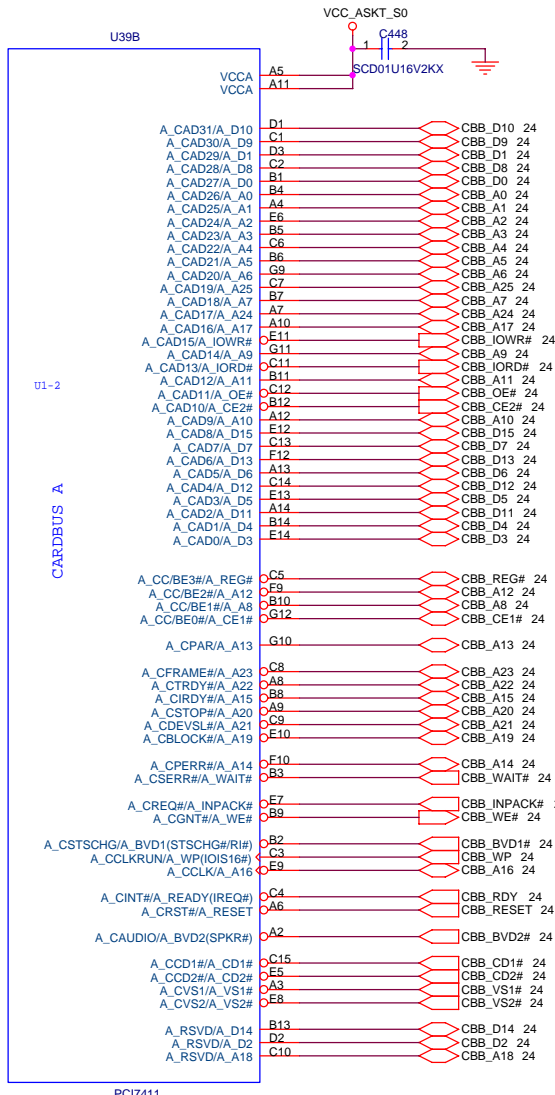
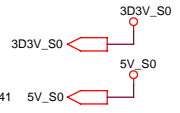
HM1-SE  
TI  
update  
sepc.

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wj Rd., Hsichih,  
Taipet Hsien 221, Taiwan, R.O.C.

Title: TI SNC1Q21 (1 of 2)

Size: A3 Document Number: Leopard Rev: -4

Date: Monday, February 28, 2005 Sheet: 22 of 41



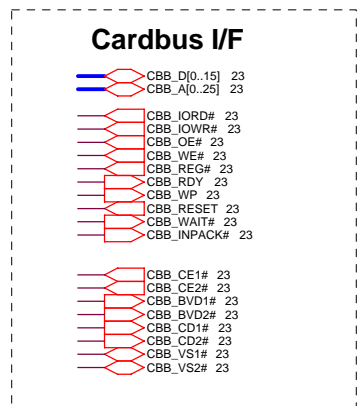
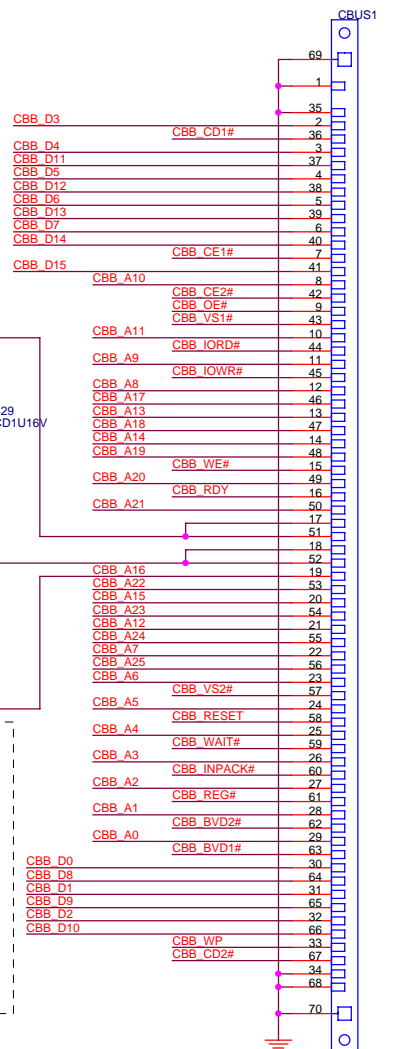
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wd Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI PCI7411 GHK (2 of 2)**

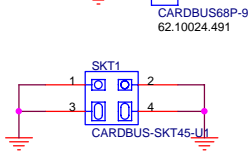
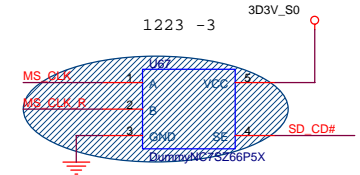
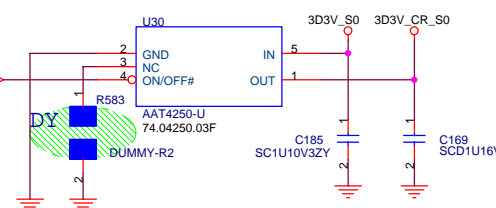
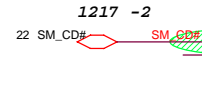
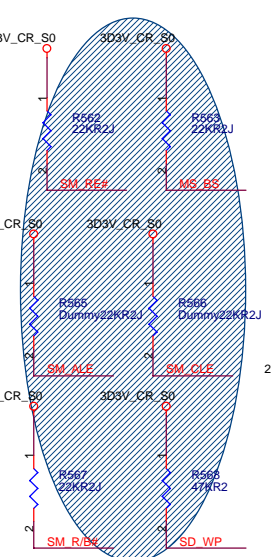
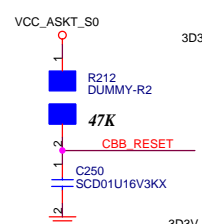
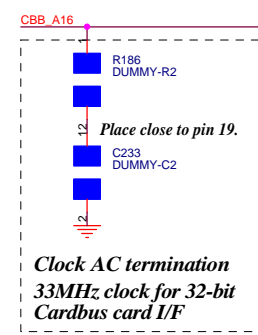
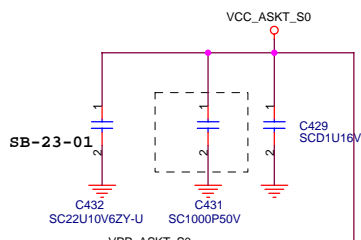
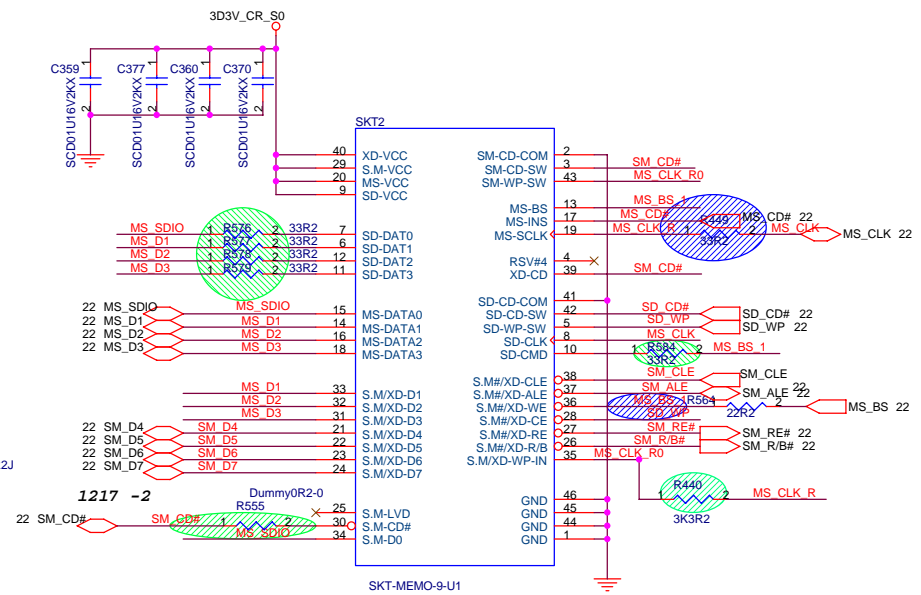
Size: A3 Document Number: **Leopard** Rev: -4

Date: Monday, February 28, 2005 Sheet: 23 of 41

# PCMCIA Socket



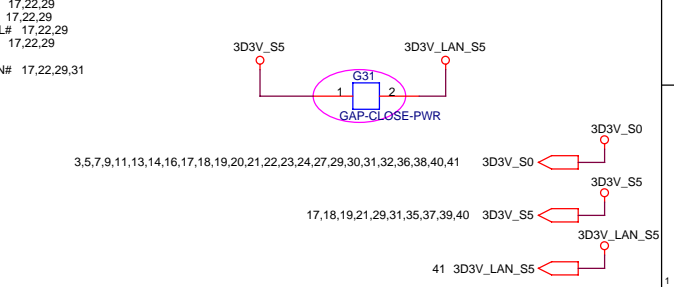
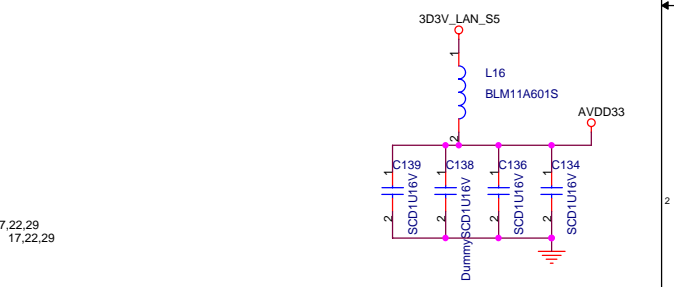
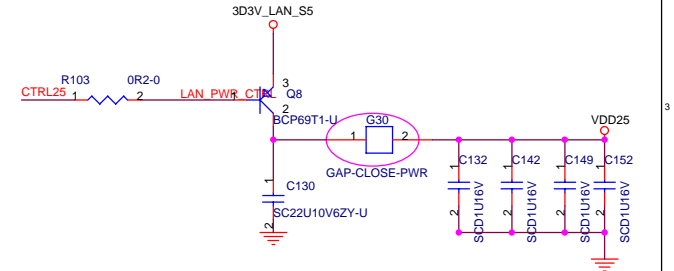
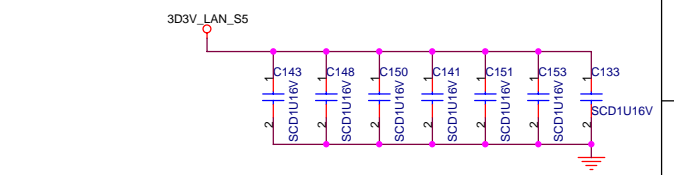
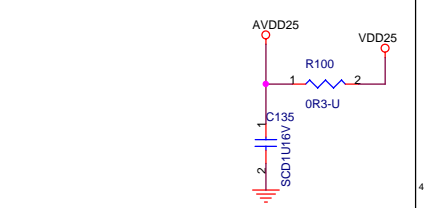
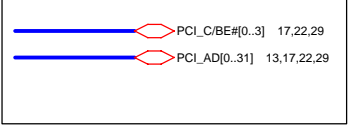
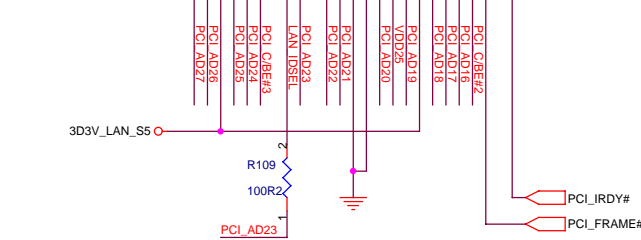
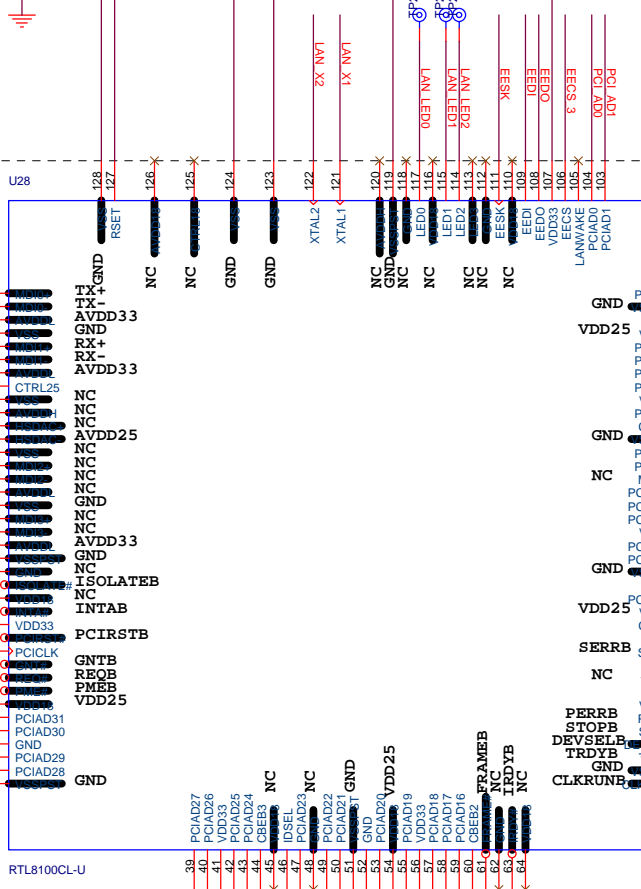
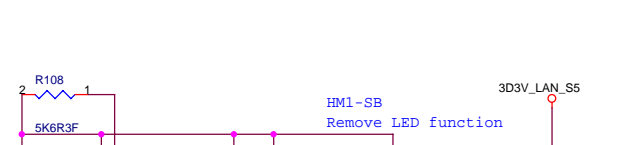
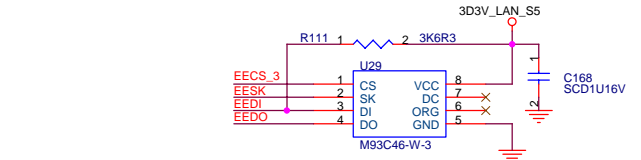
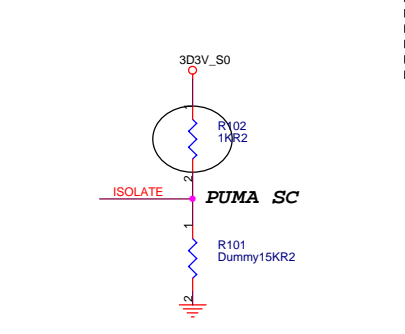
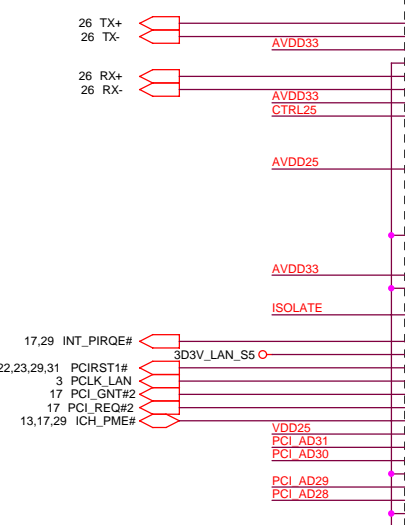
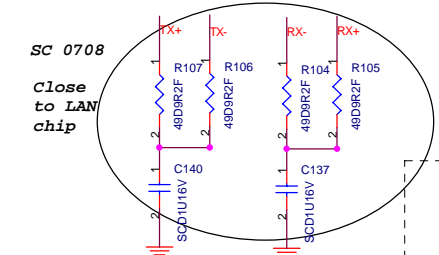
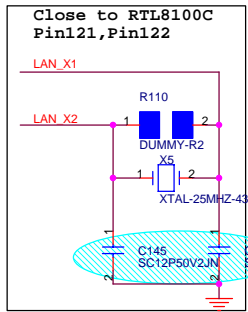
# 6 in 1 Connector



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title PCMCIA SLOT/ CARDBUS SKT			
Size A3	Document Number	Rev -4	
<b>Leopard</b>			
Date: Monday, February 28, 2005			
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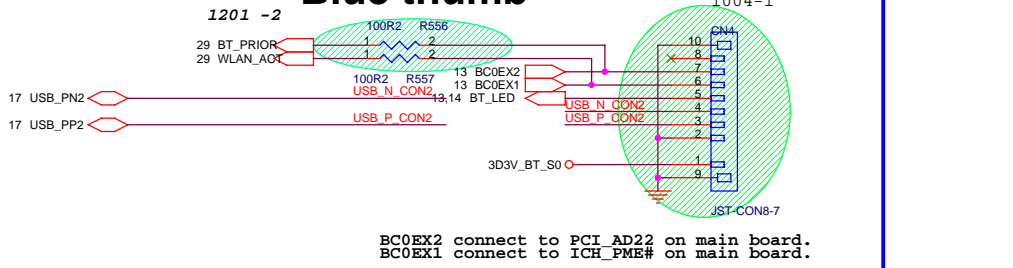
Title: **LAN RTL8100C**

Size: A3 Document Number: **Leopard** Rev: **-4**

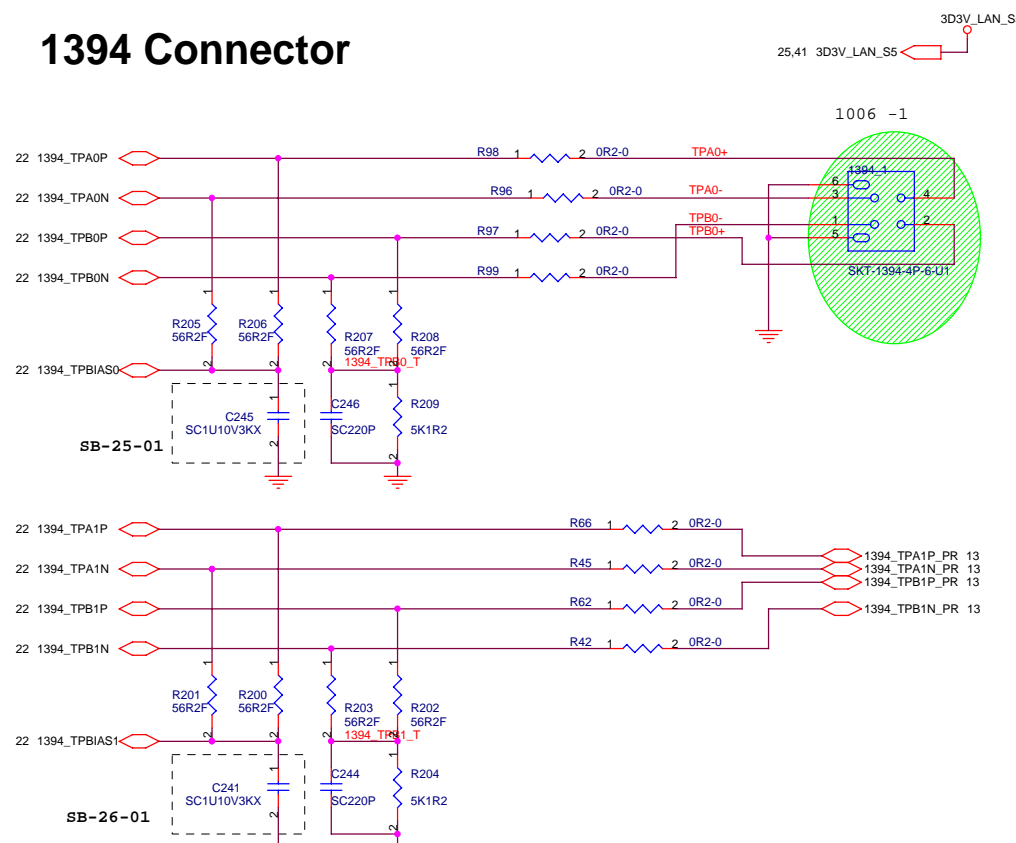
Date: Monday, February 28, 2005 Sheet: 25 of 41

# Blue thumb

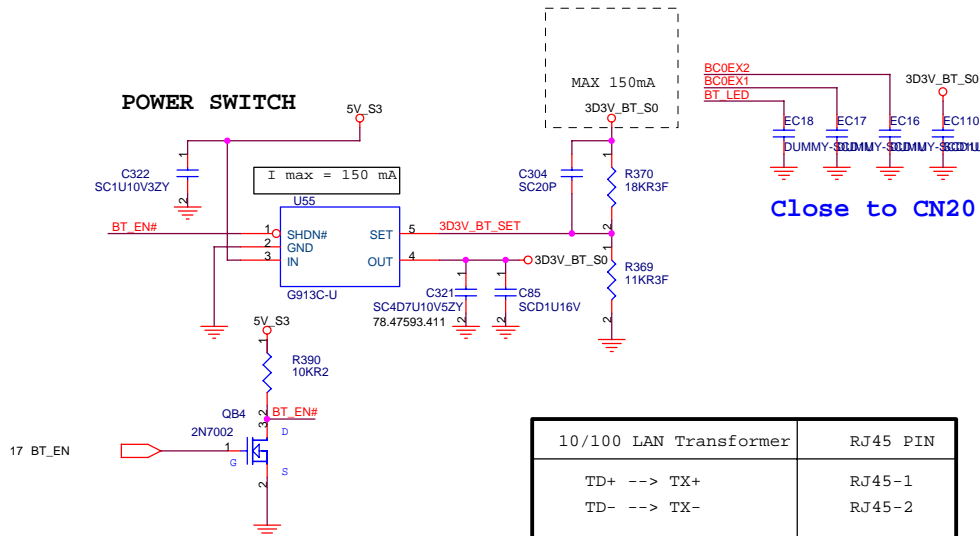
Place on bottom side



# 1394 Connector

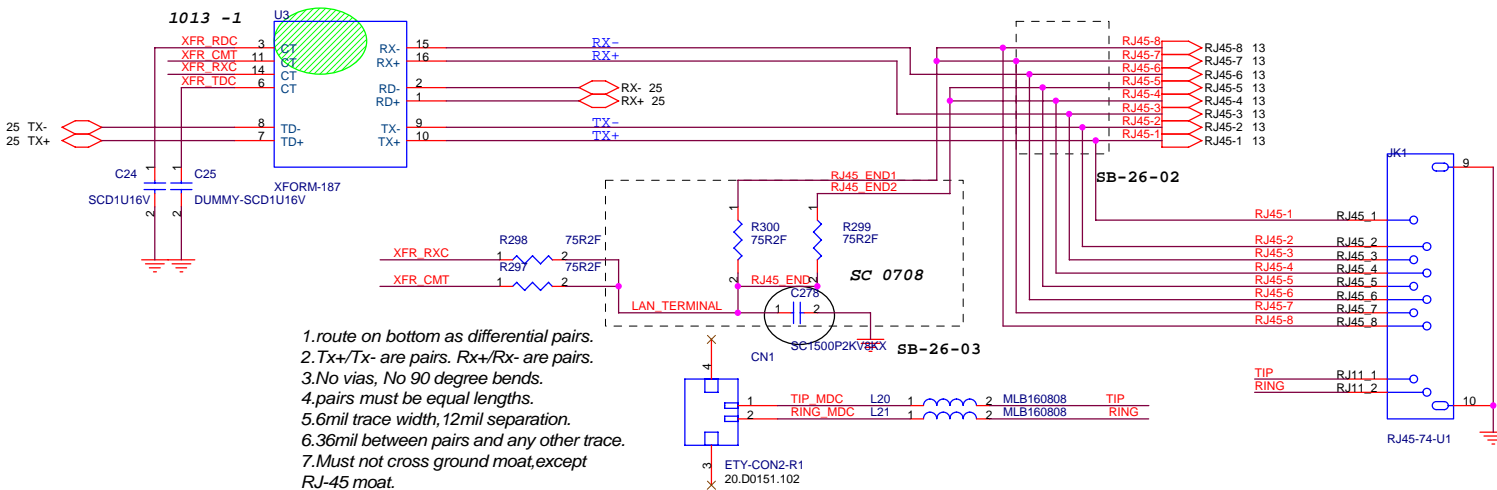


## POWER SWITCH



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

## 10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

These components near to chip side.

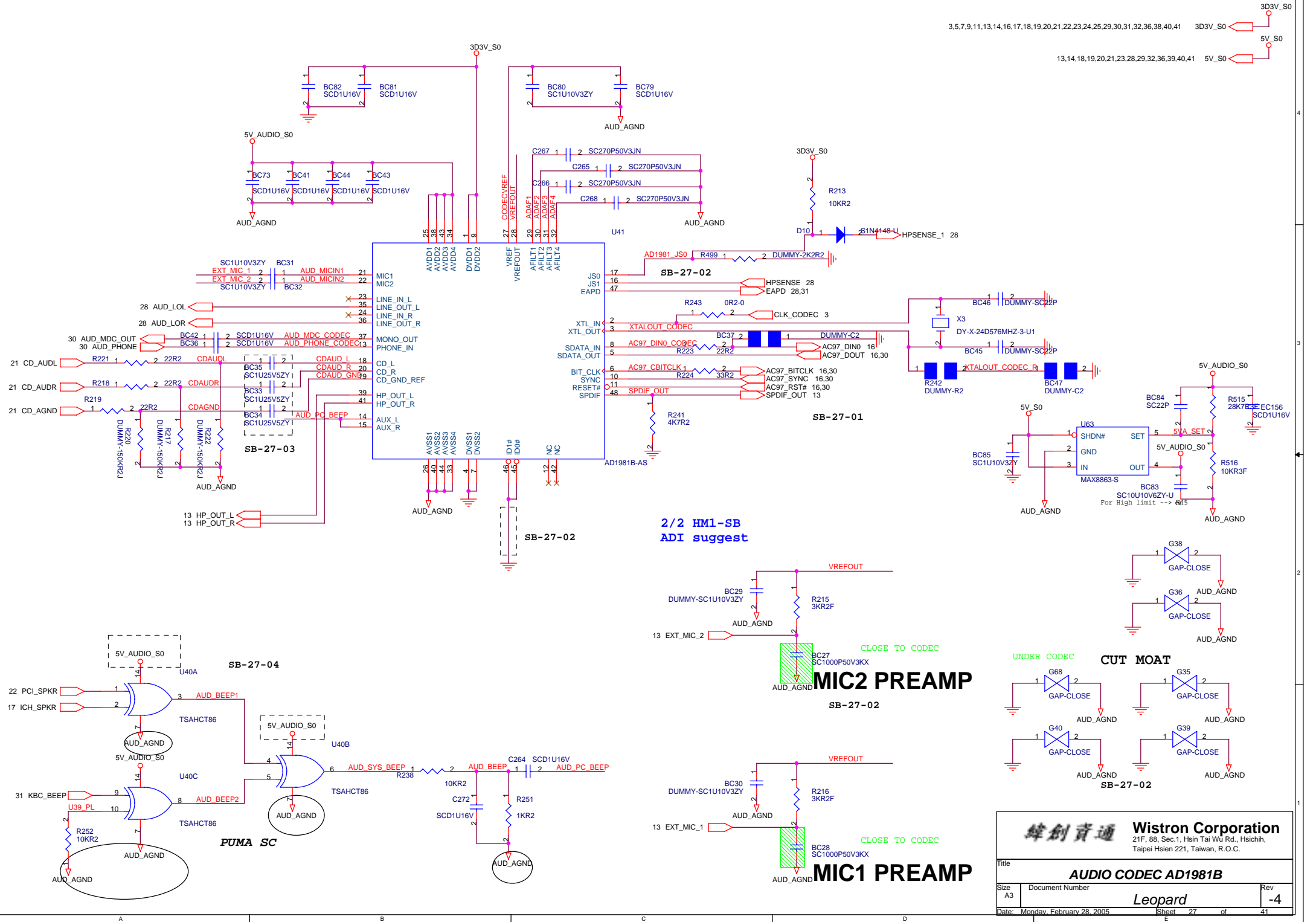
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN / 1394 Connector

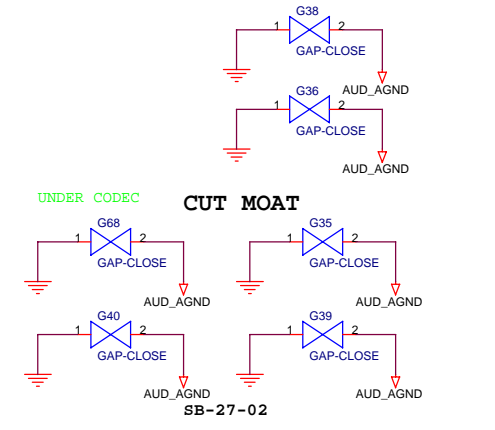
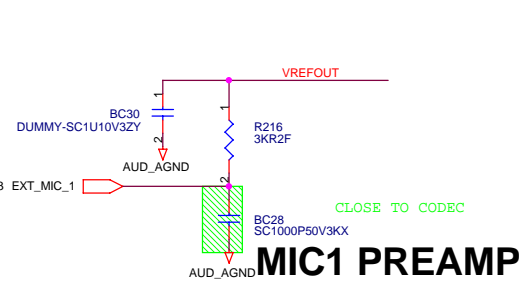
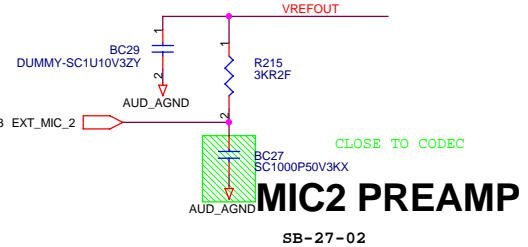
Size: A3 Document Number: Leopard Rev: -4

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3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,29,30,31,32,36,38,40,41 3D3V\_S0  
 13,14,18,19,20,21,23,28,29,32,36,39,40,41 5V\_S0



2/2 HM1-SB  
 ADI suggest



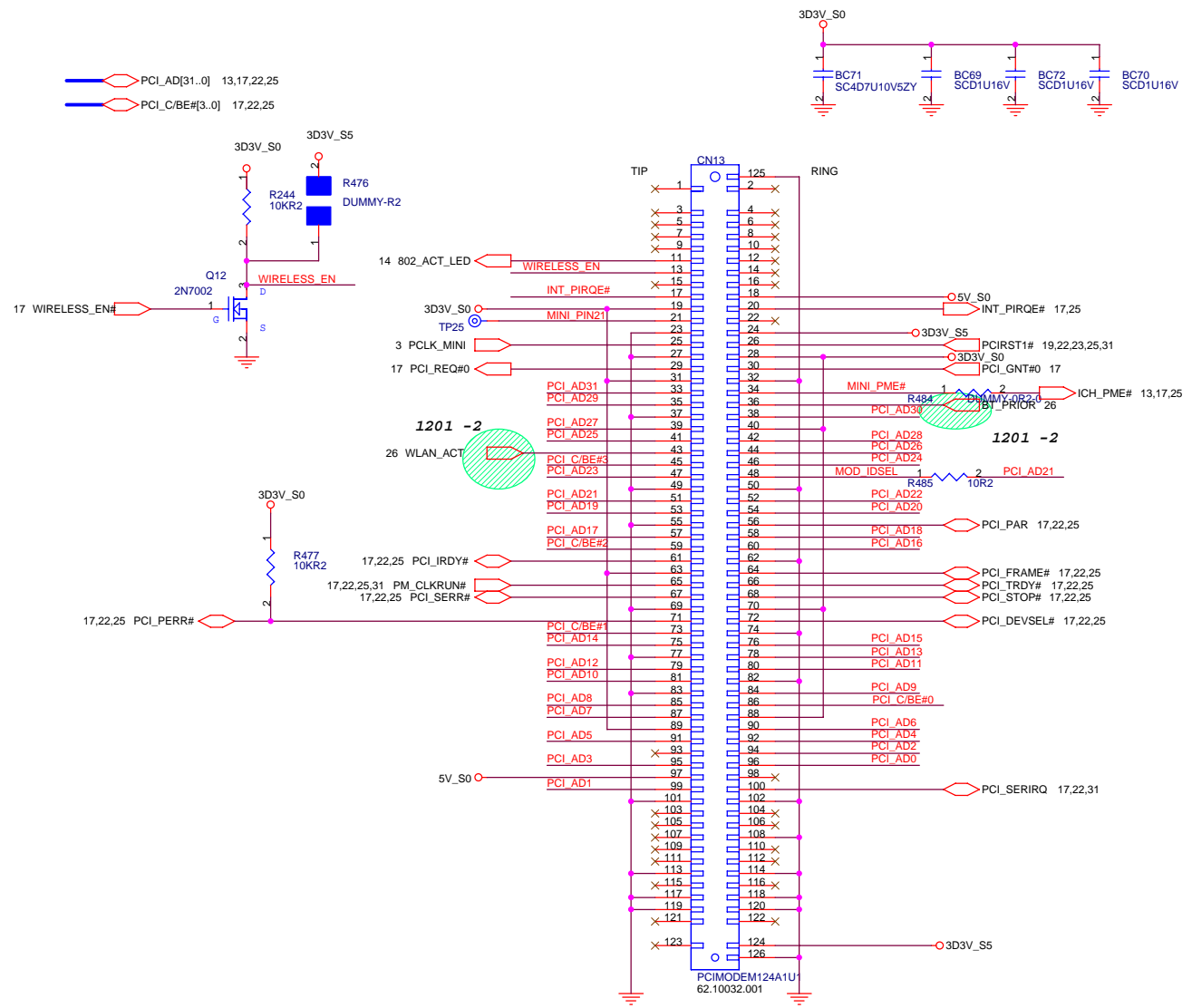
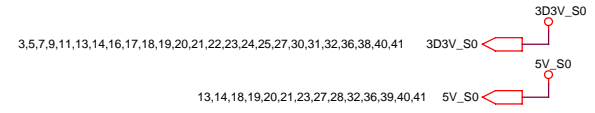
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wj Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC AD1981B**

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Date: Monday, February 28, 2005		Sheet: 27 of 41



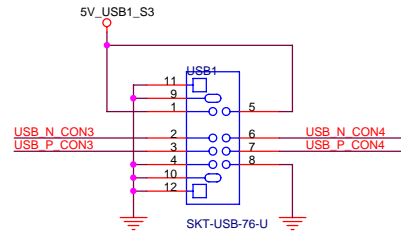
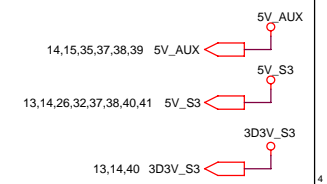
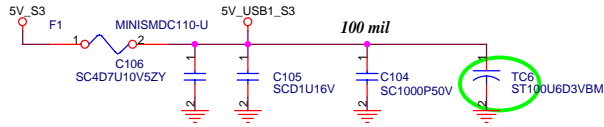
# MINI-PCI



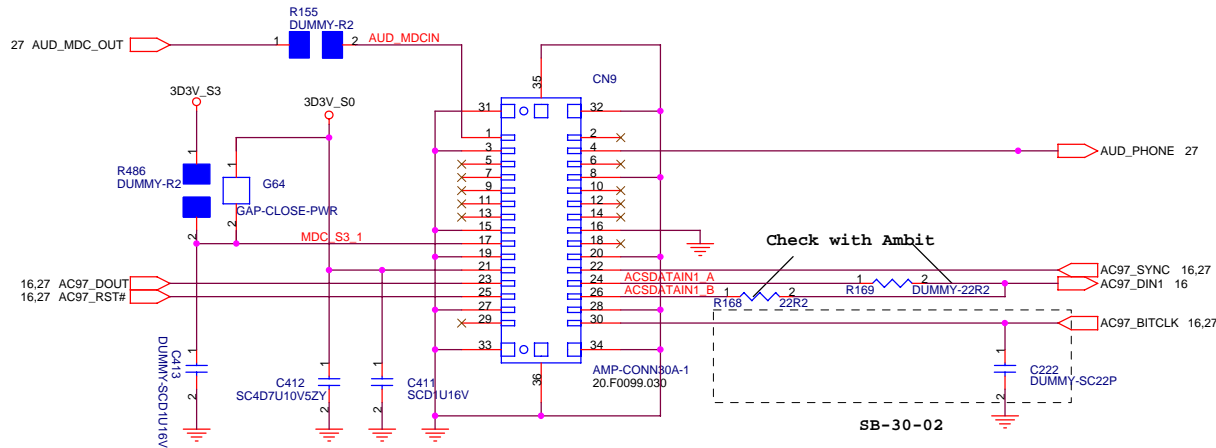
The symbol use 2nd source  
 The P/N is the main source  
 Main source: 62.10032.001  
 2nd source: 62.10032.031

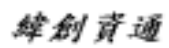
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MINI-PCI</b>	
Title MINI-PCI	Document Number <b>Leopard</b>
Size A3	Rev -4
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# USB POWER



# MDC Connector

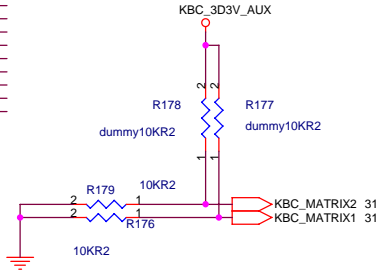
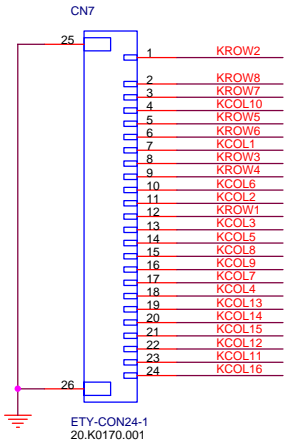


 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB / MDC CONN.</b>	
Title Size A3	Document Number <b>Leopard</b>
Date: Monday, February 28, 2005	Sheet 30 of 41
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# INTERNAL KEYBOARD CONNECTOR

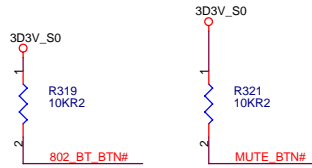
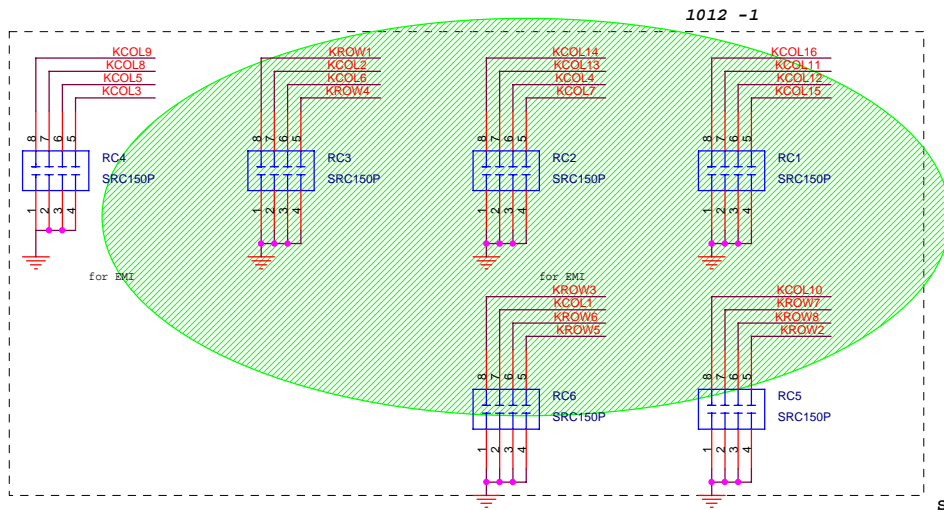
KROW[1..8] 31    KCOL[1..16] 31



the matrix table for PCB

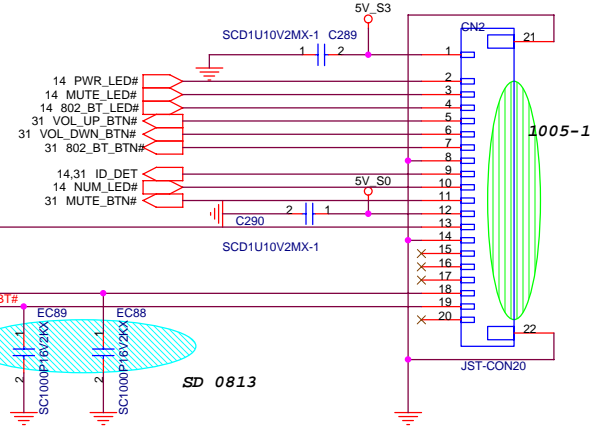
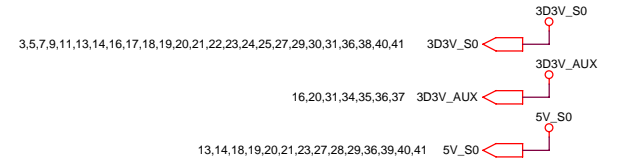
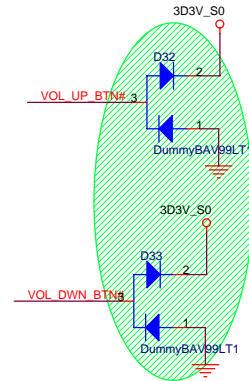
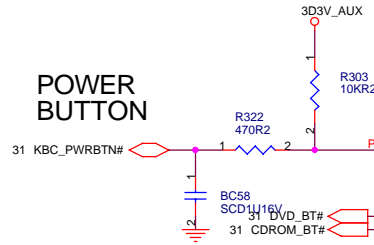
KBC_MATRIX2, KBC_MATRIX1		
PA	PR	
FF	00	01
DF	10	11

	NONE Quick Play	Quick Play
MATRIXID1#	0	1

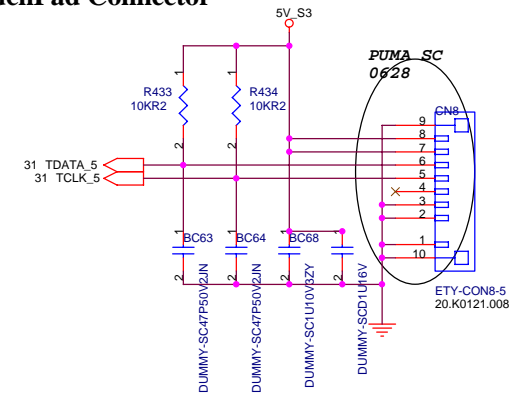


# LAUNCH Board

## POWER BUTTON

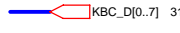
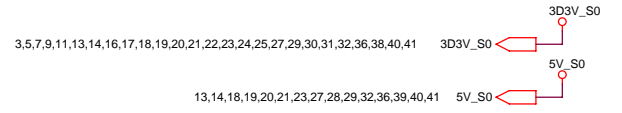


## TouchPad Connector

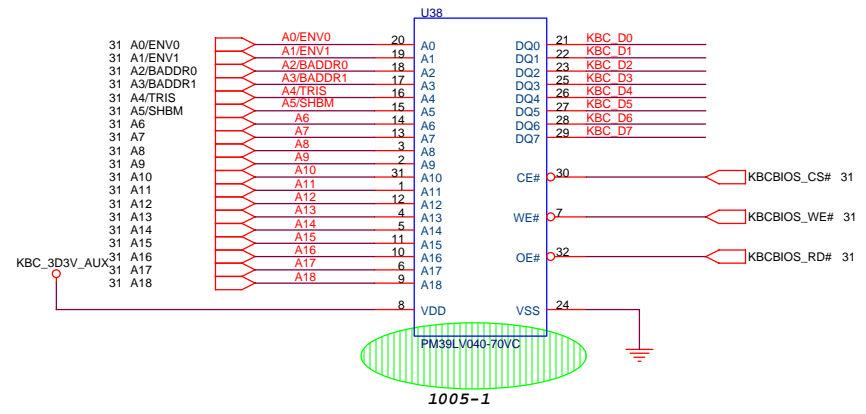


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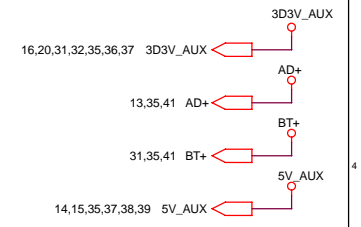
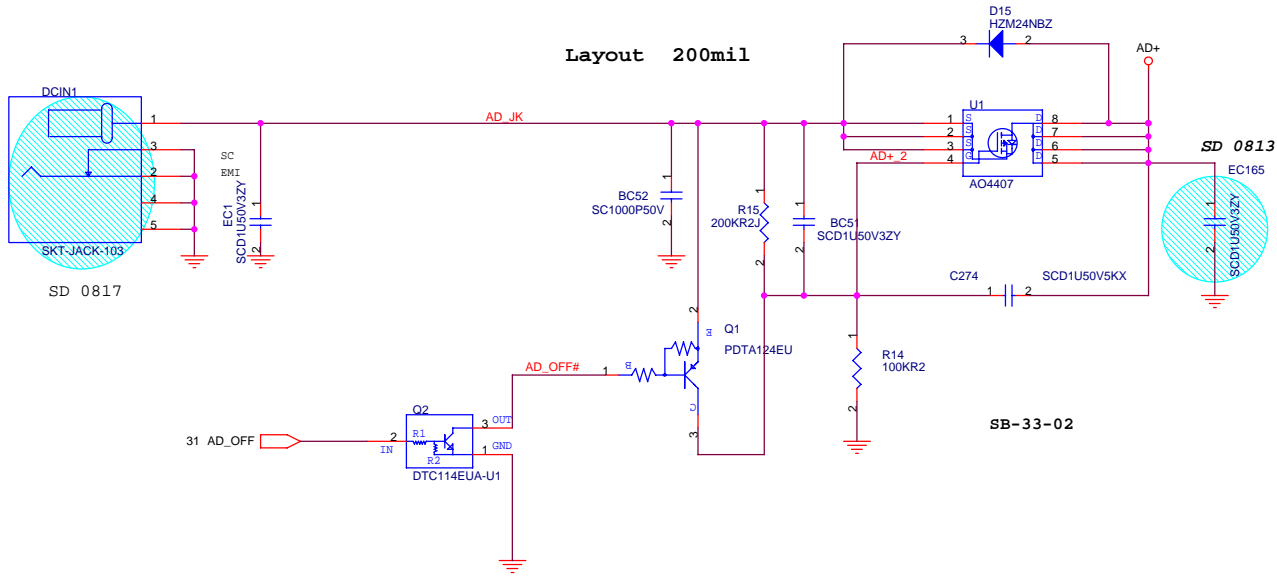


**512KB Flash**

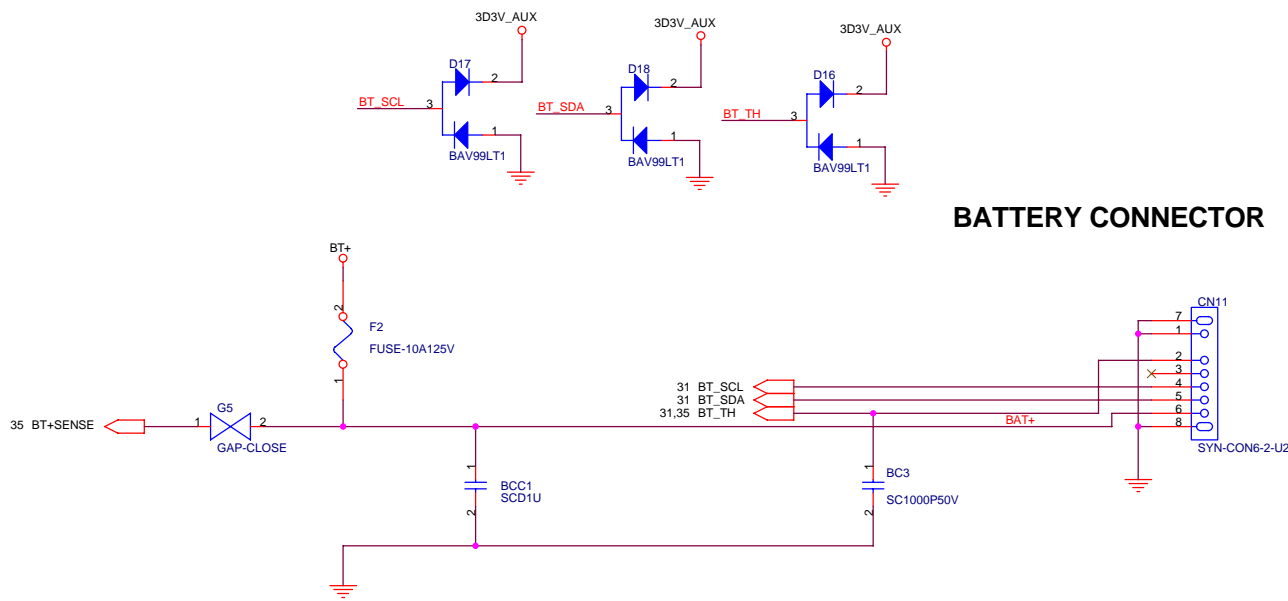


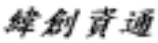
# Adaptor in to generate DCBATOUT

Layout 200mil



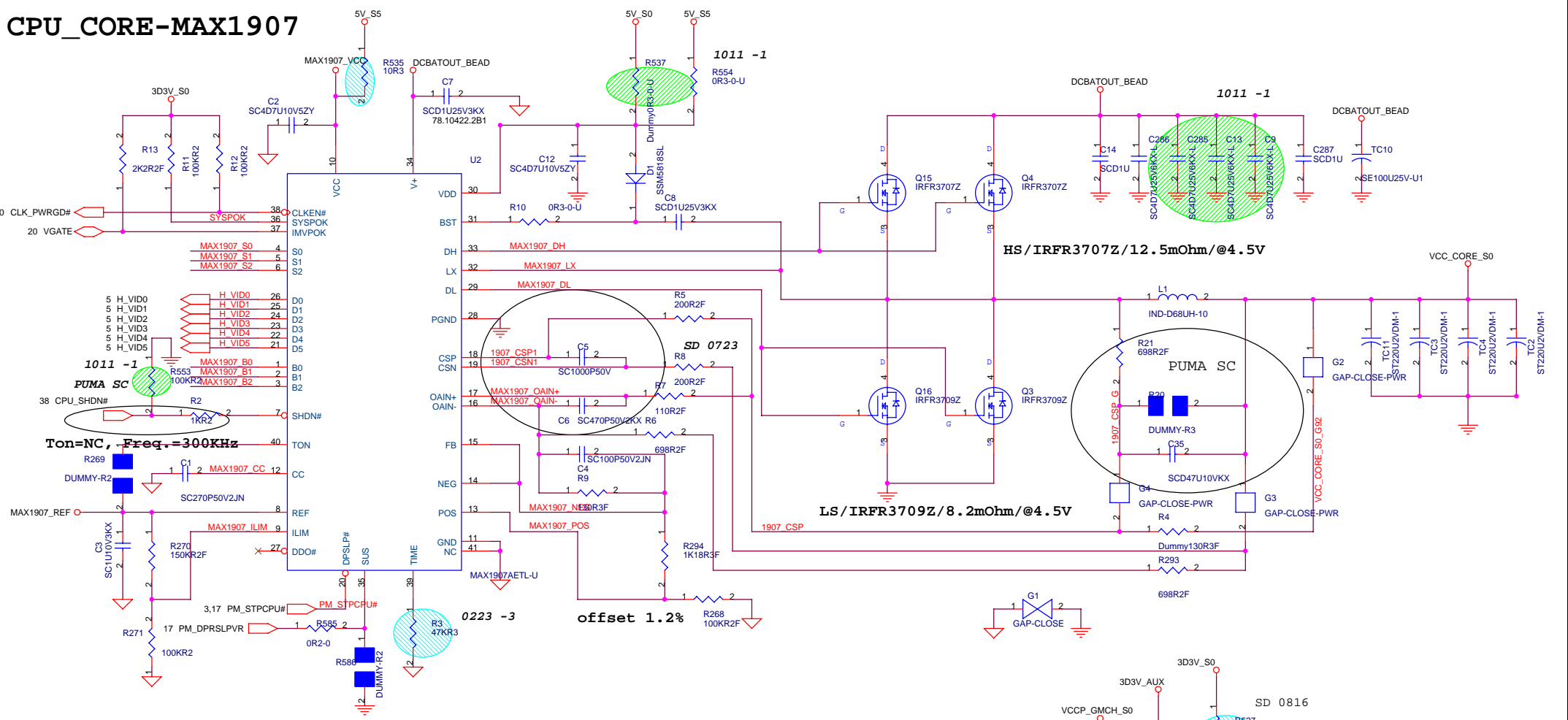
## BATTERY CONNECTOR



 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>Adaptor/ Battery conn.</b>	
Size	Document Number
A3	<b>Leopard</b>
Date: Monday, February 28, 2005	Rev -4
Sheet 34	of 41



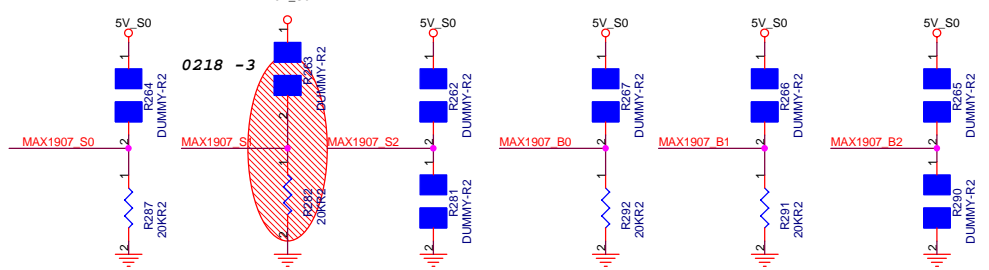
# CPU\_CORE-MAX1907



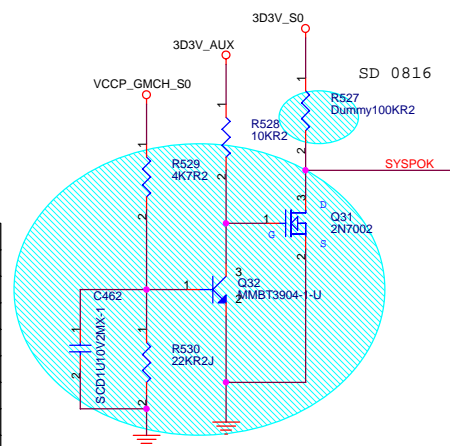
OCP=30A, Vally current = 27.5A,  
Vilim=550mV(55mVp-p\*10)

Deeper Sleep Voltage : 0.748V  
, S0=L, S1=H, S2=Open,  
5V\_S0

Boot-up Voltage : 1.2V  
, B0=L, B1=L, B2=Open



VID							Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	



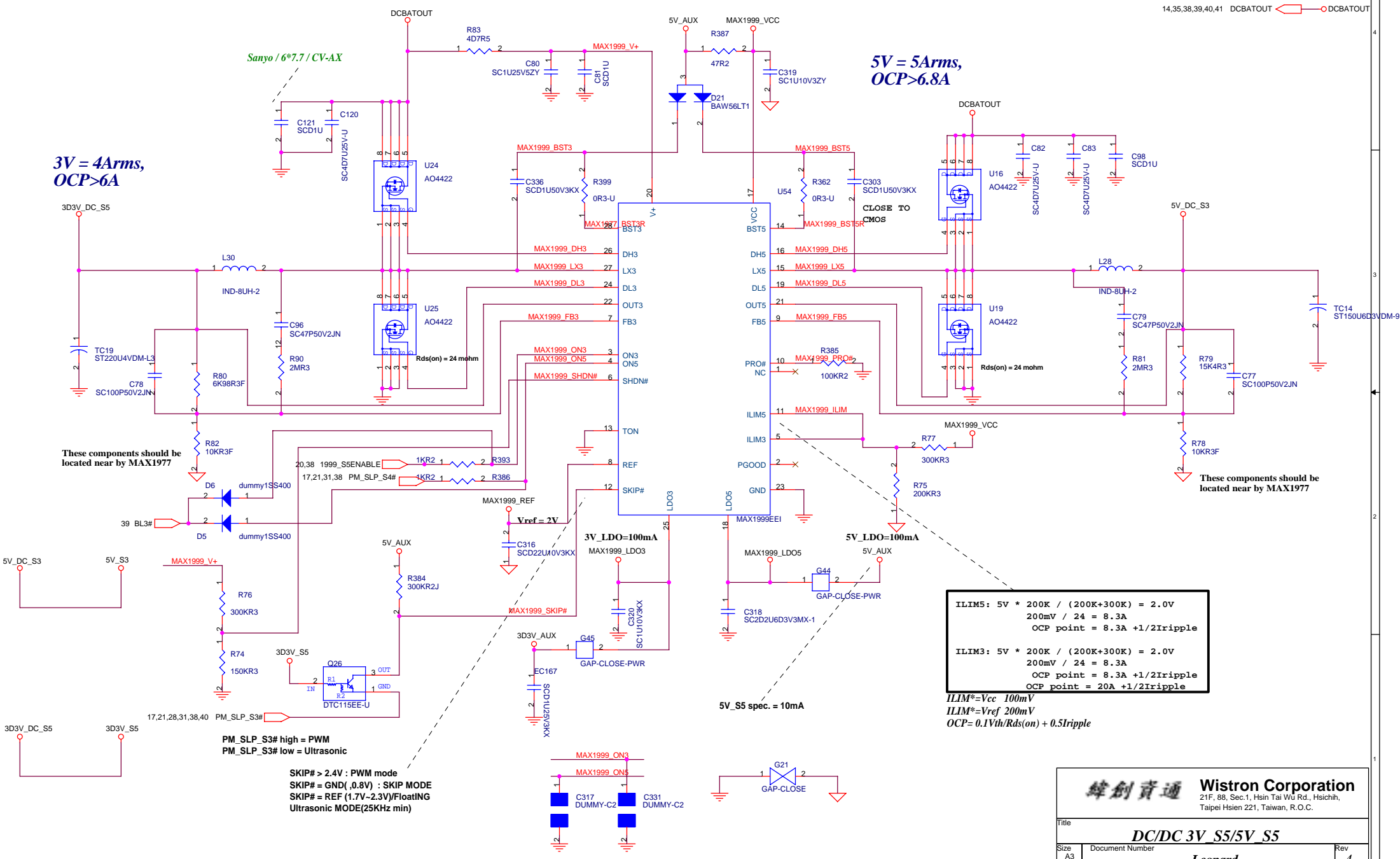
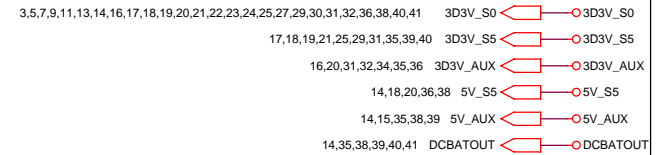
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wj Rd., Hsichih,  
Taipai Hsien 221, Taiwan, R.O.C.

Title: **IMVP IV-CPU POWER-MAX1907**

Size: A3 Document Number: **Leopard** Rev: -4

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# SYSTEM DC/DC 3D3V\_S5 / 5V\_S5



**3V = 4Arms,  
OCP>6A**

**5V = 5Arms,  
OCP>6.8A**

These components should be located near by MAX1977

These components should be located near by MAX1977

**ILIM5:**  $5V * 200K / (200K+300K) = 2.0V$   
 $200mV / 24 = 8.3A$   
**OCP point = 8.3A +1/2Iripple**

**ILIM3:**  $5V * 200K / (200K+300K) = 2.0V$   
 $200mV / 24 = 8.3A$   
**OCP point = 8.3A +1/2Iripple**

*ILIM\*=Vcc 100mV*  
*ILIM\*=Vref 200mV*  
*OCP= 0.1Vth/Rdson + 0.5Iripple*

5V\_S5 spec. = 10mA

PM\_SLP\_S3# high = PWM  
 PM\_SLP\_S3# low = Ultrasonic

SKIP# > 2.4V : PWM mode  
 SKIP# = GND(,0.8V) : SKIP MODE  
 SKIP# = REF (1.7V~2.3V)/FloatNG  
 Ultrasonic MODE(25KHz min)

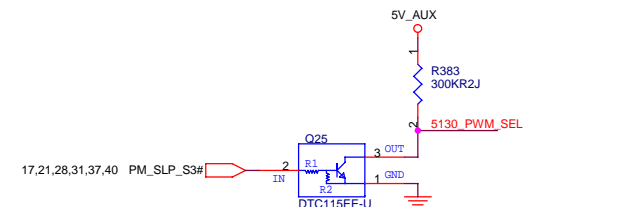
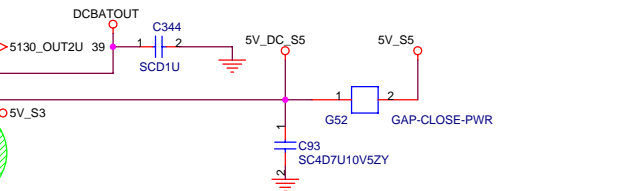
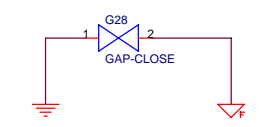
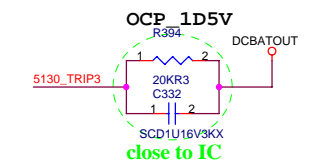
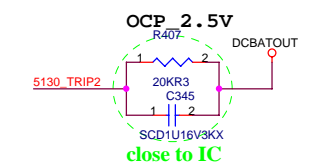
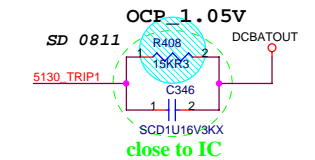
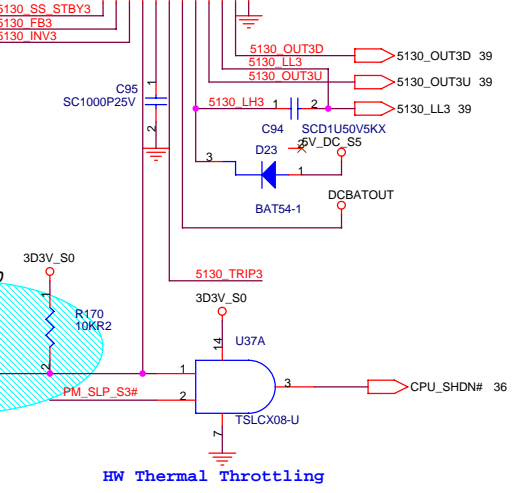
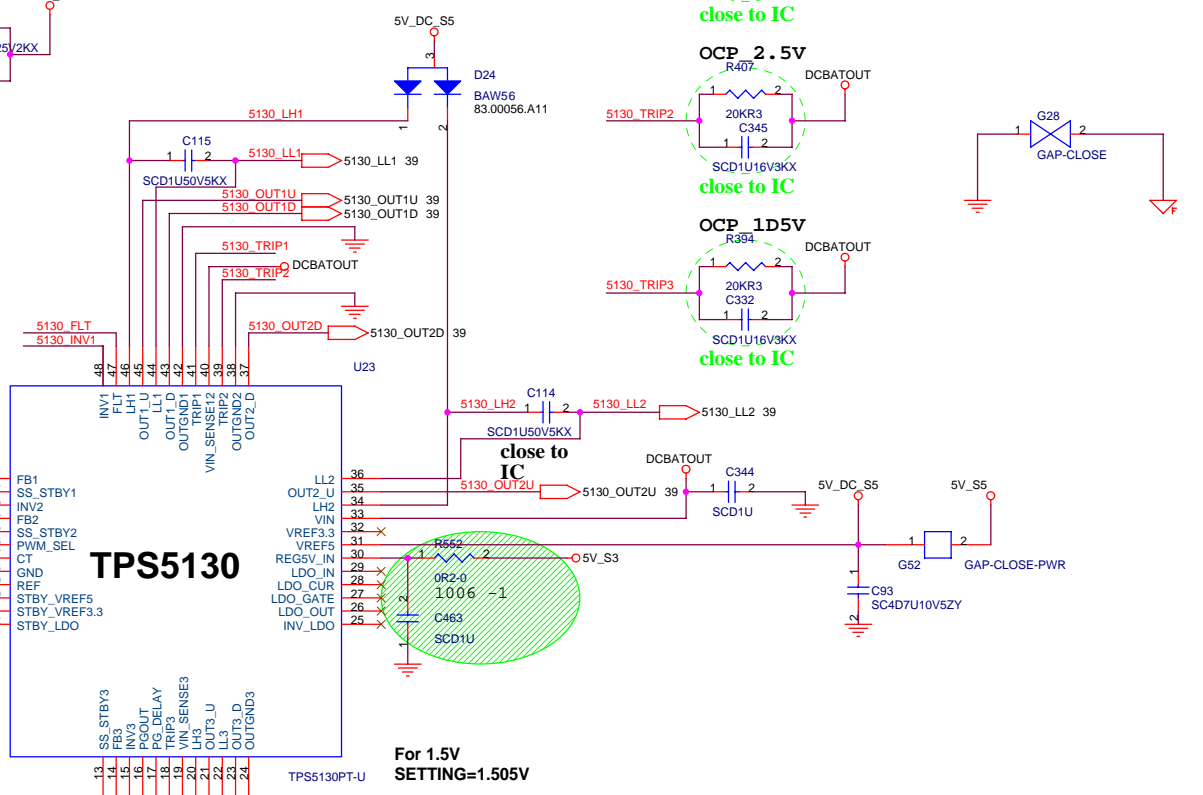
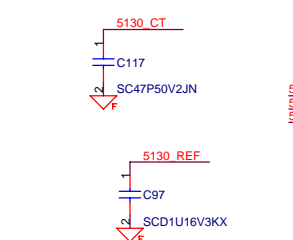
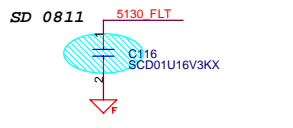
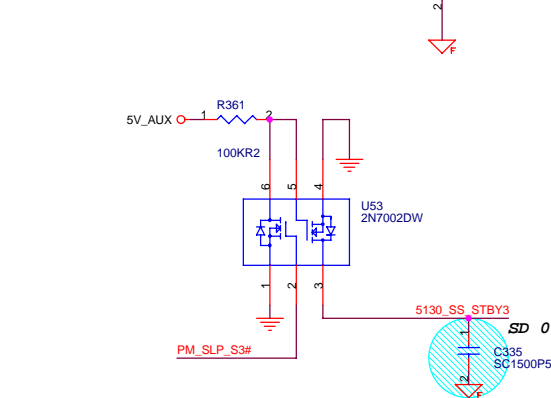
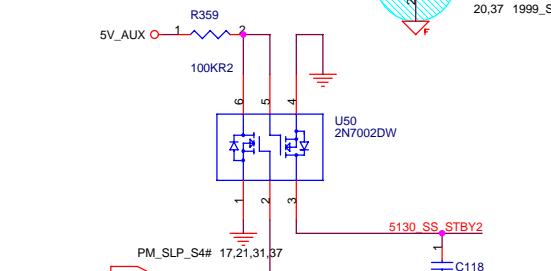
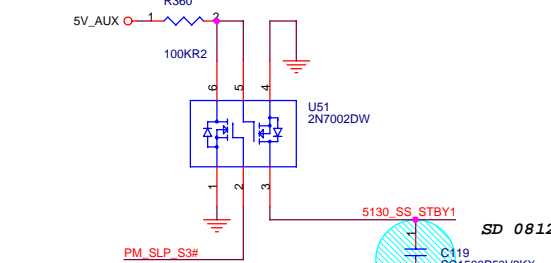
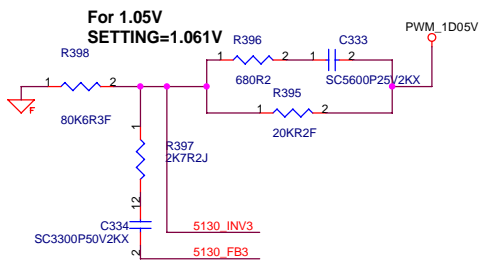
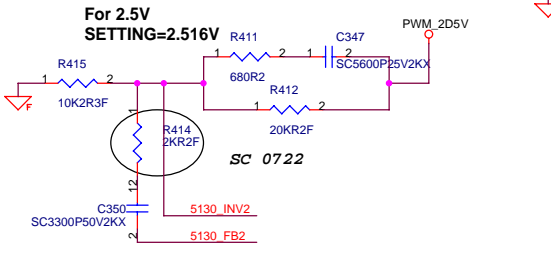
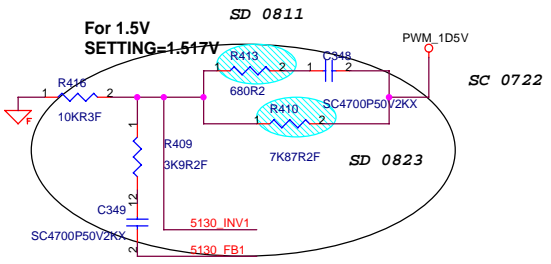
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Title: **DC/DC 3V\_S5/5V\_S5**

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# TI TPS5130 for 2.5V, 1.5V, 1.05V.

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

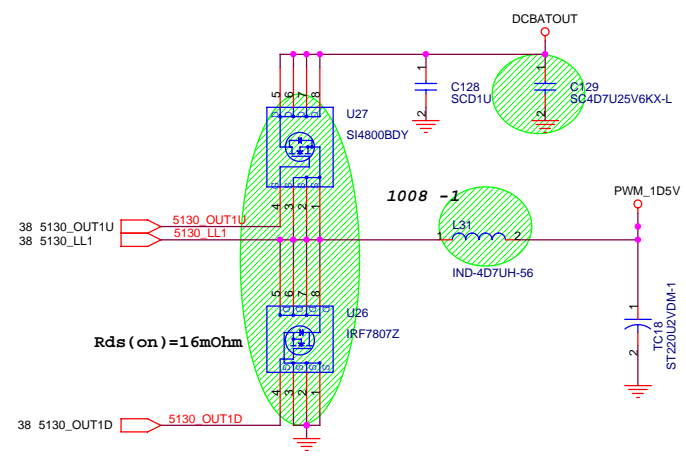


HW Thermal Throttling

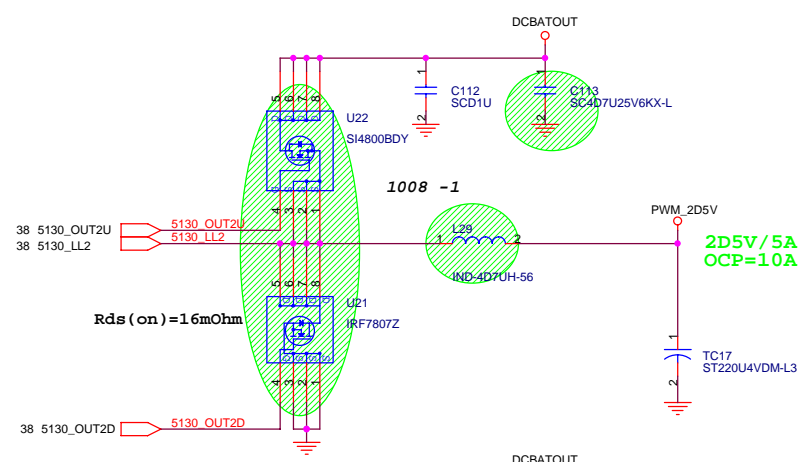
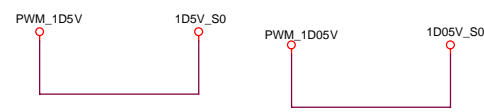
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Title <b>DC/DC 2D5V/1D5V/1D05V</b>	
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# TI TPS5130 for 2.5V, 1.5V, 1.05V

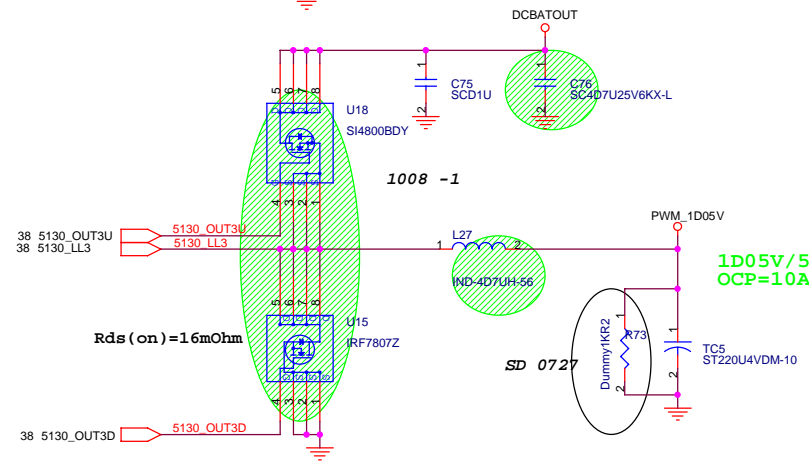
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



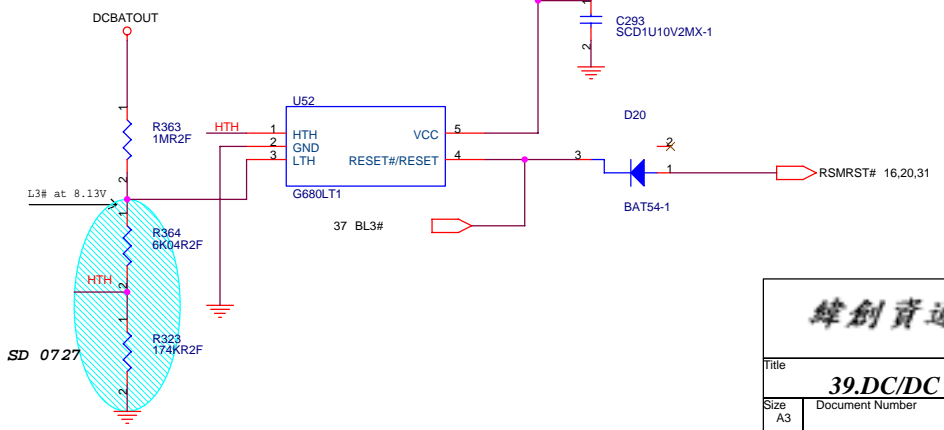
1D5V/5A  
OCP=10A



2D5V/5A  
OCP=10A

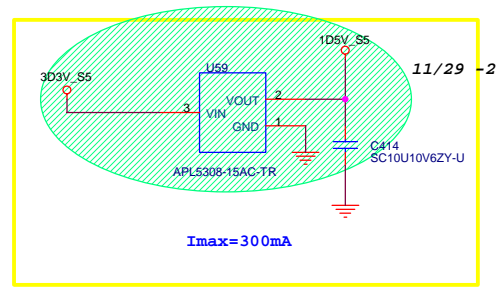


1D05V/5A  
OCP=10A

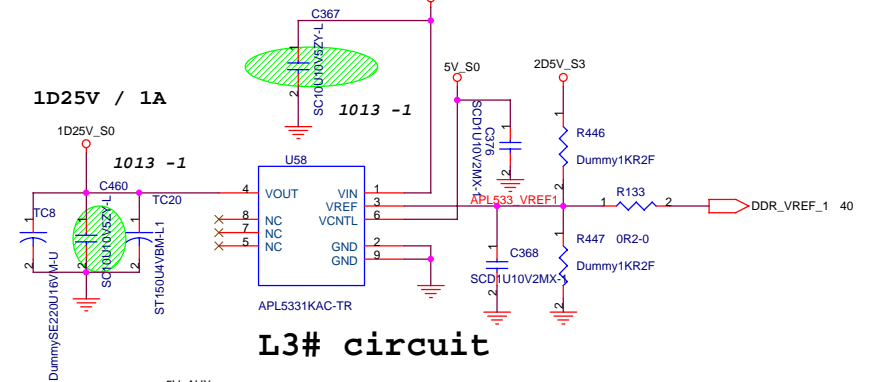


L3# at 8.13V

## 1.5V\_S5 (For ICH6)



Power budget: 1.25V/2.2Apeak (For DDR1\_VTT)



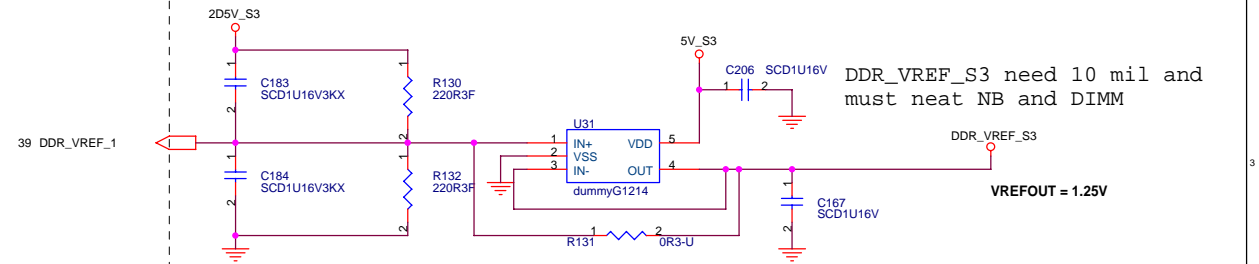
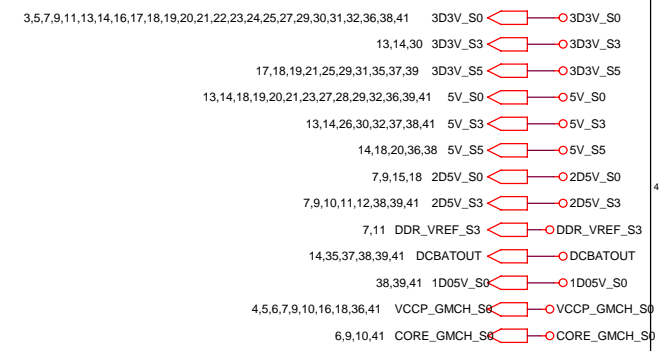
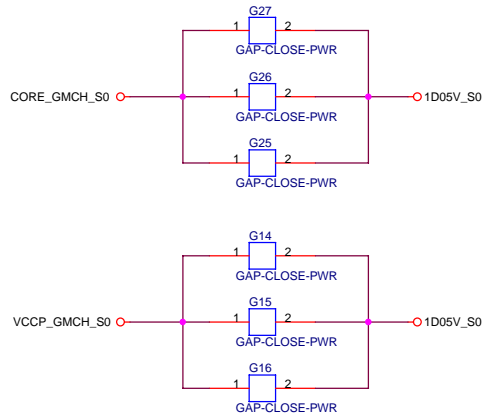
L3# circuit

- 14,35,37,38,40,41 DCBATOUT
- 17,18,19,21,25,29,31,35,37,40 3D3V\_S5
- 14,15,35,37,38 5V\_AUX
- 18 1D5V\_S5
- 7,9,10,11,12,38,40,41 2D5V\_S3
- 13,14,18,19,20,21,23,27,28,29,32,36,40,41 5V\_S0
- 12 1D25V\_S0

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Title		
<b>39.DC/DC 2D5V/1D5V/1D05V-2</b>		
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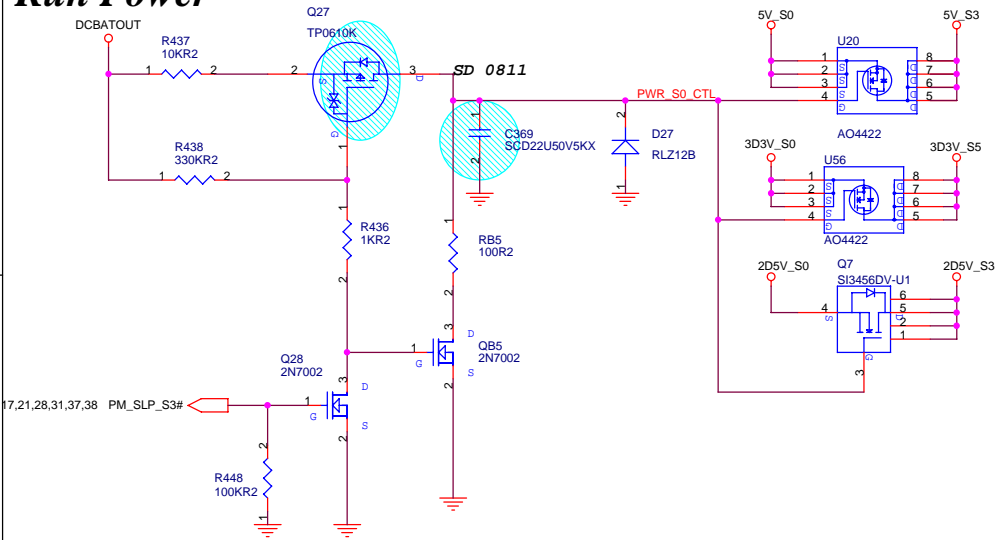
# FOR GMCH Power



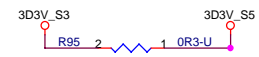
# FOR DDR Power

# Run Power

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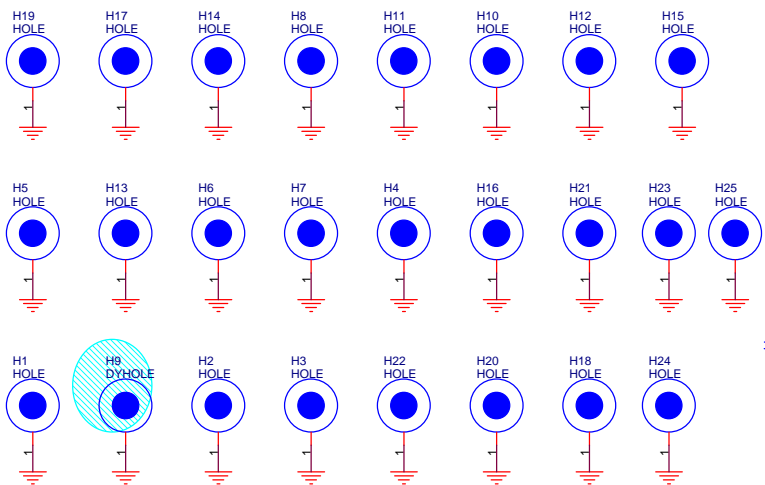
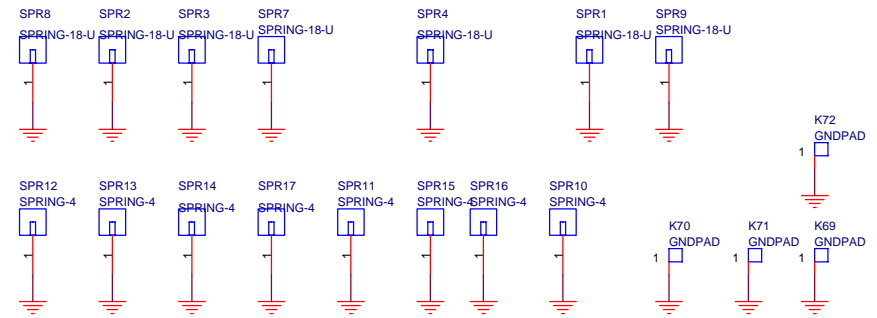
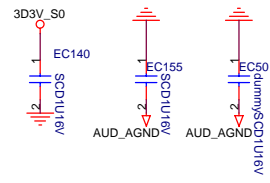
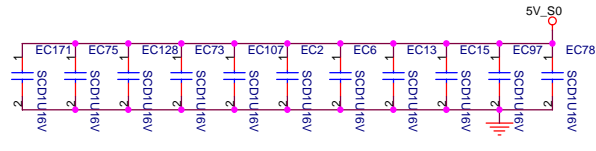
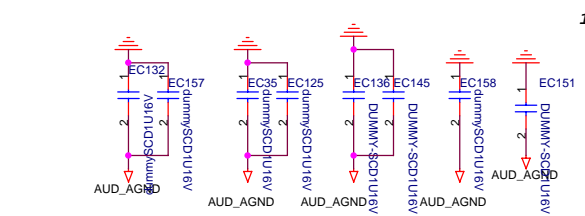
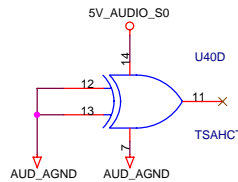
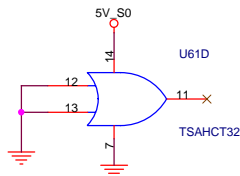


# Suspend Power

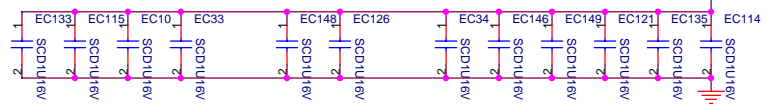
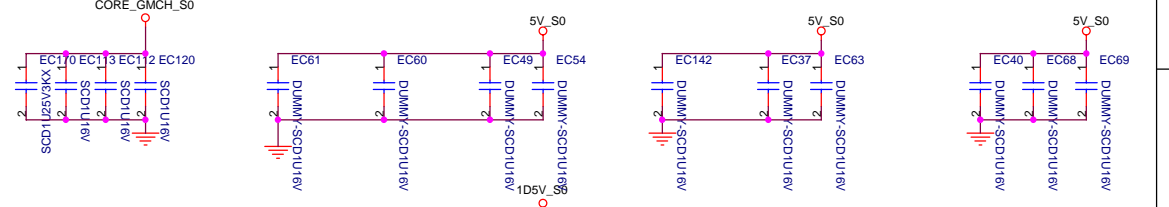
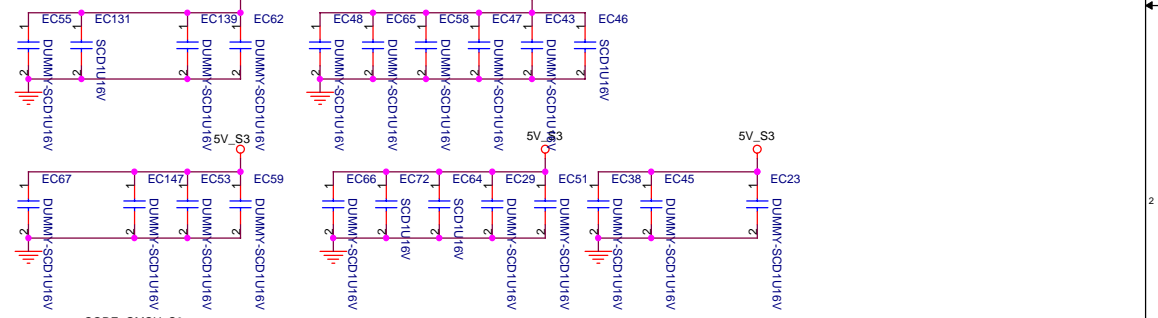
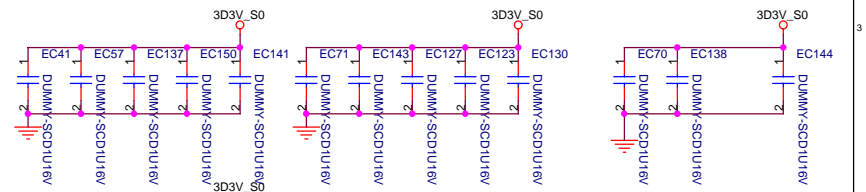
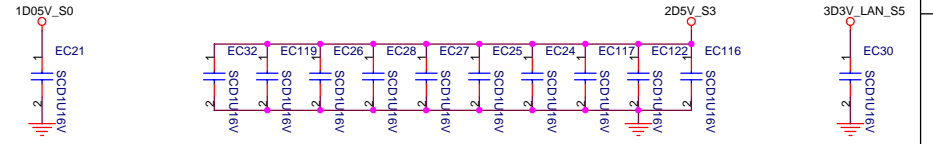
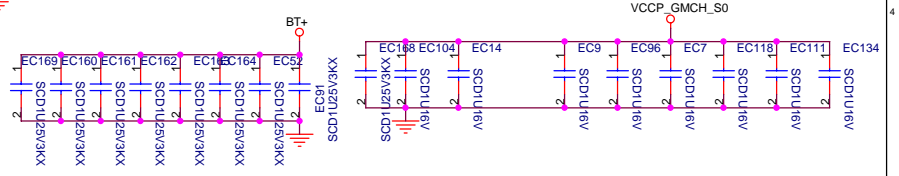
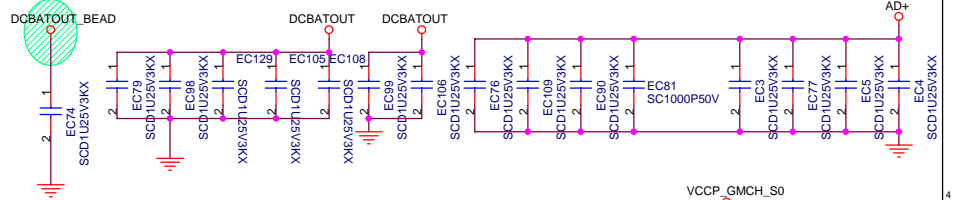


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Title: **MISC & EMI**

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